Panasonic

PROGRAMMABLE CONTROLLER

FP7 High-speed Counter Unit

User's Manual

WUME-FP7HSC-02

2014.6 | panasonic.net/id/pidsx/global

Safety Precautions

Observe the following notices to ensure personal safety or to prevent accidents.
To ensure that you use this product correctly, read this User's Manual thoroughly before use.
Make sure that you fully understand the product and information on safety.
This manual uses two safety flags to indicate different levels of danger.

WARNING

If critical situations that could lead to user's death or serious injury is assumed by mishandling of the product.

-Always take precautions to ensure the overall safety of your system, so that the whole system remains safe in the event of failure of this product or other external factor.
-Do not use this product in areas with inflammable gas. It could lead to an explosion.
-Exposing this product to excessive heat or open flames could cause damage to the lithium battery or other electronic parts.

CAUTION

If critical situations that could lead to user's injury or only property damage is assumed by mishandling of the product.

-To prevent excessive exothermic heat or smoke generation, use this product at the values less than the maximum of the characteristics and performance that are assured in these specifications.
-Do not dismantle or remodel the product. It could cause excessive exothermic heat or smoke generation.
-Do not touch the terminal while turning on electricity. It could lead to an electric shock.
-Use the external devices to function the emergency stop and interlock circuit.
-Connect the wires or connectors securely.
The loose connection could cause excessive exothermic heat or smoke generation.
-Do not allow foreign matters such as liquid, flammable materials, metals to go into the inside of the product. It could cause excessive exothermic heat or smoke generation.
-Do not undertake construction (such as connection and disconnection) while the power supply is on. It could lead to an electric shock.

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Introduction

Thank you for buying a Panasonic product. Before you use the product, please carefully read the installation instructions and the users manual, and understand their contents in detail to use the product properly.

Types of Manual

- There are different types of users manual for the FP7 series, as listed below. Please refer to a relevant manual for the unit and purpose of your use.
- The manuals can be downloaded on our website: http://industrial.panasonic.com/ac/e/dl_center/manual/ .

Unit name or purpose of use	Manual name	Manual code
FP7 Power Supply Unit	FP7 CPU Unit Users Manual (Hardware)	WUME-FP7CPUH
FP7 CPU Unit	FP7 CPU Unit Command Reference Manual	WUME-FP7CPUPGR
	FP7 CPU Unit Users Manual (Logging Trace Function)	WUME-FP7CPULOG
	FP7 CPU Unit Users Manual (Security Function)	WUME-FP7CPUSEC
Instructions for Built-in LAN Port	FP7 CPU Unit Users Manual (LAN Port Communication)	WUME-FP7LAN
Instructions for Built-in COM Port	FP7 series Users Manual (SCU communication)	WUME-FP7COM
FP7 Extension Cassette (Communication) (RS-232C/RS485 type)		
FP7 Extension Cassette (Communication) (Ethernet type)	FP7 series Users Manual (Communication cassette Ethernet type)	WUME-FP7CCET
FP7 Extension (Function) Cassette Analog Cassette	FP7 Analog Cassette Users Manual	WUME-FP7FCA
FP7 Digital Input/Output Unit	FP7 Digital Input/Output Unit Users Manual	WUME-FP7DIO
FP7 Analog Input Unit	FP7 Analog Input Unit Users Manual	WUME-FP7AIH
FP7 Analog Output Unit	FP7 Analog Output Unit Users Manual	WUME-FP7AOH
FP7 High-speed counter Unit	FP7 High-speed counter Unit Users Manual	WUME-FP7HSC
FP7 Pulse Output Unit	FP7 Pulse Output Unit Users Manual	WUME-FP7PG
FP7 Positioning Unit	FP7 Positioning Unit Users Manual	WUME-FP7POSP
FP7 Serial Communication Unit	FP7 series Users Manual (SCU communication)	WUME-FP7COM
PHLS System	PHLS System Users Manual	WUME-PHLS
Programming Software FPWIN GR7	FPWIN GR7 Introduction Guidance	WUME-FPWINGR7

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Unit Functions and Restrictions

1.1 Unit Functions and How They Work

1.1.1 Functions of Unit

■ Two or four-point 4 MHz/signed 32-bit high-speed counters are provided.

- High-speed counting of input signals is available up to the maximum frequency 4 MHz (16MHz for 2-phase 4 multiple). It is selectable from 2-phase input (phase differential input), individual input or direction detection input in accordance with input devices such as an encoder and sensor.

■ 24 VDC, 12 VDC, 5 VDC inputs and line driver input are available.

- The count input circuit supports both an open collector output and a line driver output (Differential output: Equivalent to AM26LS31).

■ Selectable from ring counter or linear counter.

- Both the ring counter and linear counter are available. The Z phase of an encoder can be used as count reset timing in the both methods.

■ Frequency measurement function and Rotation speed measurement function are provided.

- Frequencies are automatically measured in the unit from count values. Also, the rotation speed is automatically measured from count values and the pulse number for one rotation. The calculation results are directly stored in unit memories, thus no calculation using ladder programs is needed.

■ The count of internal clocks is available.

- Internal clocks occurred in the unit can be selected as count input signals. Timing measurement is ahievable with high accuracy of the maximum resolution 0.25 μs. The selectable internal clocks are 0.25 μs (4 MHz), 1 μs (1 MHz), 10 μs (100 kHz) and 100 μs (10 kHz).

■ Capture function and Sampling capture function are provided.

- It is possible to store the count value at the moment of the occurrence of a trigger assinged to a control signal. The count value independent of the scan time of PLC can be confirmed.
- The capture function is used to execute capturing at the leading and trailing edges of control signals, and the sampling capture function is used to execute capturing every sampling time (T [ms]) by signla input.
- Buffer function is added, which can save up to 60 captured data. (Available form High-speed counter unit Ver.1.2.)

■ 14 counter operations by input signals (input z signal, control signal and output relay (Y relay).

1) Reset operation at rising edge, 2) Reset operation at trailing edge, 3) Positive logic reset operation,
4) Negative logic reset operation, 5) Preset operation at rising edge, 6)Preset operation at trailing edge,
7) Positive logic preset operation, 8) Negative logic preset operation, 9)Positive logic enable operation,
10) Negative logic enable operation, 11) Positive logic enable operation and reset operation at rising edge,
12) Negative logic enable operation and reset operation at trailing edge,
13) Positive logic enable operation and preset operation at rising edge,
14) Negative logic enable operation and preset operation at trailing edge

■ **Forced ON/OFF of external output relays (Y relays) is available.**

- External output relays can be forcibly turned on/off by the monitoring function of a programming tool or ladder program. It is usable for checking wirings when setting up the system.

■ **Band comparison function and Target value match comparison function are provided.**

- Two types of comparison functions are selectable for count values.
- In the band comparison function, a maximum of 16 band comparison conditions (max. 16 sets of upper and lower limits) can be specified for each counter. A maximum 16 outputs can be turned on/off for each comparison condition. It is also possible to turn on an external output relay when the count value is in the range of the specified condition.
- In the target value match comparison function, a maximum of 16 target value match comparison conditions can be specified for each counter. A maximum of 16 outputs are set or reset for each comparison condition in accordance with the count direction when the count value reaches a target value. It is also possible to turn on external output relays.

■ **Programmable output ON function**

- When using the band comparison function, the ON timing characteristics of external output relays can be changed.
  ON timing delay [1 ms ~ 1000 ms]: Delays the ON timing of output.
  ON hold time [1 ms ~ 1000 ms]: Holds the on state of output during a specified time.
  The ON timing delay and the ON hold time can be used in combination.

■ **Input time constant (Noise filter)**

- The noise filter function is available which sets the input time constant to reduce noises of input A, B and Z signals of each counter, and control signal lines.

Input signal name	Noise filter type
Input A signal, input B signal (The same time constant for the both signals)	0.1 µs (2 MHz), 0.2 µs (1 MHz), 0.5 µs (500 kHz), 1.0 µs (250 kHz), 2.0 µs (100 kHz), 10.0 µs (10 kHz)
Input Z signal	0.1 µs (2 MHz), 0.2 µs (1 MHz), 0.5 µs (500 kHz), 1.0 µs (250 kHz), 2.0 µs (100 kHz), 10.0 µs (10 kHz)
Control signal	2 µs, 5µs, 10 µs, 20 µs, 50 µs, 100 µs, 500 µs, 1 ms, 2 ms, 5 ms, 10 ms

1.1.2 Unit Type and Product Number

Name		Product No.
FP7 High-speed counter unit	2-ch type	AFP7HSC2T
	4-ch type	AFP7HSC4T

1.2 Restrictions on Combinations of Units

1.2.1 Restrictions on Power Consumption

The internal current consumption of the unit is as follows. Make sure that the total current consumption is within the capacity of the power supply with consideration of all other units used in combination with this unit.

Name		Product No.	Current consumption
FP7 High-speed counter unit	2-ch type	AFP7HSC2T	65 mA or less
	4-ch type	AFP7HSC4T	65 mA or less

1.2.2 Applicable Versions of FPWIN GR7 and Units

For using the high-speed counter unit, the following versions of FPWIN GR7 and units are required.

Item	Applicable version
Programmingn tool software FPWIN GR7	Ver.1.2 or later
FP7 CPU unit	Ver.1.2 or later
FP7 Positioning unit	For using the interrupt function with the high-speed counter unit, Ver.1.1 or later is required.

1.2.3 Restrictions on Interrupt Function

- The high-speed counter unit can activate interrupt programs of CPU using comparison match flags.
- However, the units which can use the function to activate interrupt programs should be in the range of the following specifications.

■ Interrupt program specifications

Item	Specifications	
Interrupt program activation condition	Activates corresponding interrupt programs when the comparison match 0 flag and comparison match 1 flag of each channel turns on.	
No. of interrupt programs	Per 1 channel of High-speed counter unit	Max. 2 programs
	Per 1 High-speed counter unit	Max. 4 programs (2-ch type High-speed counter unit) Max. 8 programs (4-ch type High-speed counter unit)
	Per 1 CPU unit	Max. 64 programs (8 programs x 8 units)

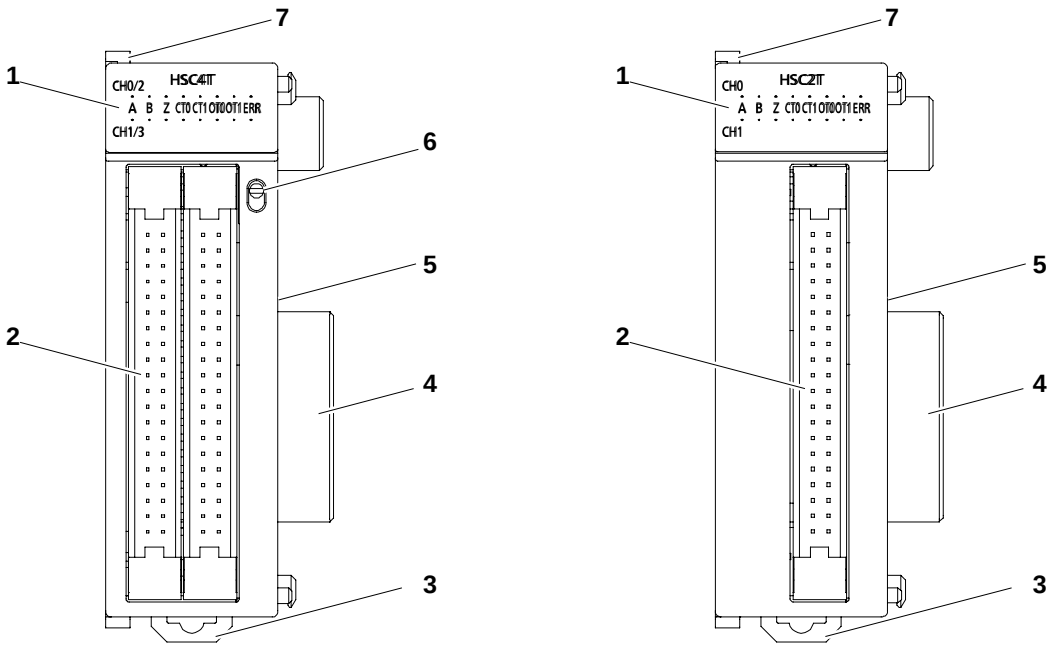
(Note 1) If interrupt occurs many times in one scan, the execution of intterupt program has priority, and the scan time will be longer.

(Note 2) If more than one interrupt activation request is made from the unit, the process will be carried out from the smallest slot number or the smallest interrupt program number.

2

Names and Functions of Parts

2.1 Names and Functions of Parts



① Operation monitor LEDs

Displays the on/off status of two channels. Use the display changeover switch to toggle between the channel number CH0/CH1 and CH2/CH3. The LEDs show the same information for each channel.

LED	Description	Color	ON	OFF	Flashing
HSC	Power supply of the unit	Blue	ON	OFF	—
A	Pulse input A signal display	Green	Displays the status of the input signal		
B	Pulse input B signal display	Green	Displays the status of the input signal		
Z	Pulse input Z signal display	Green	Displays the status of the input signal		
CT0	Control 0 signal display	Green	Positive logic	Negative logic	—
CT1	Control 1 signal display	Green	Positive logic	Negative logic	—
OT0	External output 0 signal display	Green	ON	OFF	—
OT1	External output 1 signal display	Green	ON	OFF	—
ERR	Error display	Red	If an error occurs	Normal operation	—

(Note1): The LEDs for the pulse input signals flash according to the input statuses, thus look as if they are continuously lit if the input frequencies are high.

(Note 2): The LED of each input signal indicates the status after an input time constant processing.

② Input/output connector

Connector for input and output (40 pins) (Conforms to MIL standard)

③DIN hook

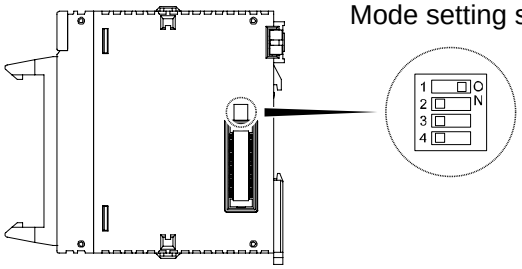
This hook is used to install the unit on a DIN rail.

④ Unit connector

Connects the internal circuits between units.

⑤ Mode setting switch

- Change the switch to use the interrupt function.
- At the factory setting, it is set to off (no interrupt function).



	Description
1	ON: Interrupt function is enabled. OFF: Interrupt function is disabled.
2	Not used
3	
4	

⑥ Display changeover switch

Toggle between the display of 0ch/1ch and that of 2ch/3ch.

⑦ Fixing hook

This hook is used to fix units.

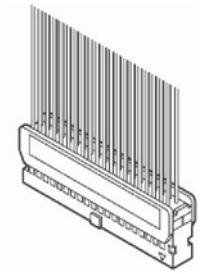
3

Wiring and Input/Output Specifications

3.1 Connection over Wire-pressed Terminal Cable

3.1.1 Specifications of Wire-pressed Terminal Cable

This is a connector that allows loose wires to be connected without removing the wires' insulation. The pressure connection tool is required to connect the loose wires.



Discrete-wire connector (40P)

Suitable wires (strand wire)

Size	Nominal cross-sectional area	Insulation thickness	Rated current
AWG#22	0.3 mm^2	1.5 to 1.1 dia.	3 A
AWG#24	0.2 mm^2		

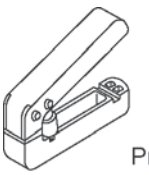
Connector for wire-pressed terminal cable (provided with the unit)

Manufacturer	Composition of parts	Unit type and required quantity	
		2-ch type	4-ch type
Panasonic made	Housing (40P)	1 x 1 set	1 x 2 sets
	Semi-cover (40P)	2 x 1 set	2 x 2 sets
	5-pin contact (for AWG 22 and AWG24)	8 x 1 set	8 x 2 sets

(Note) 1 connector set and 2 connector set are supplied with the 2-ch type unit and 4-ch type unit, respectively. If you need more connectors, purchase AFP2801 (2 sets/pack).

Pressure connection tool

Manufacturer	Product no.
Panasonic made	AXY52000FP



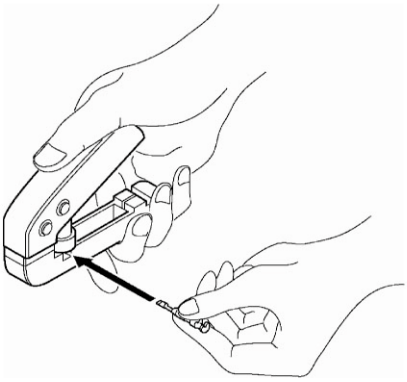
Pressure connection tool

3.1.2 Assembly of Connector for Wire-pressed Terminal Cable

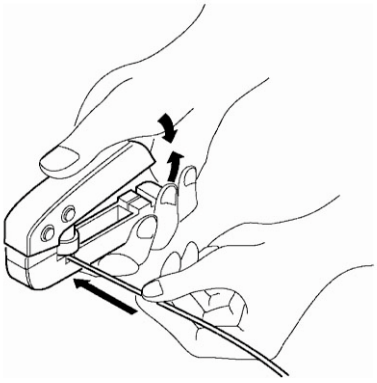
The wire end can be directly crimped without removing the wire's insulation, which saves wiring effort.

(Procedure)

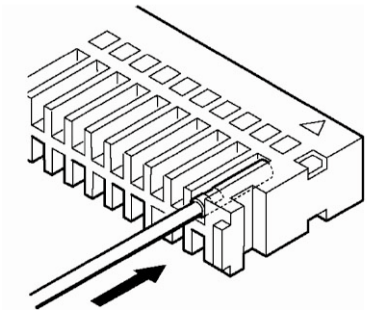
1. Bend the contact back from the carrier, and set it in the pressure connection tool.



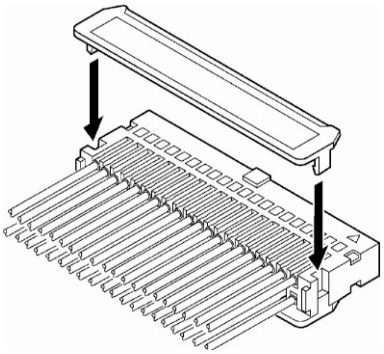
2. Insert the wire without removing its insulation until it stops, and lightly grip the tool.



3. After press fitting the wire, insert it into the housing.

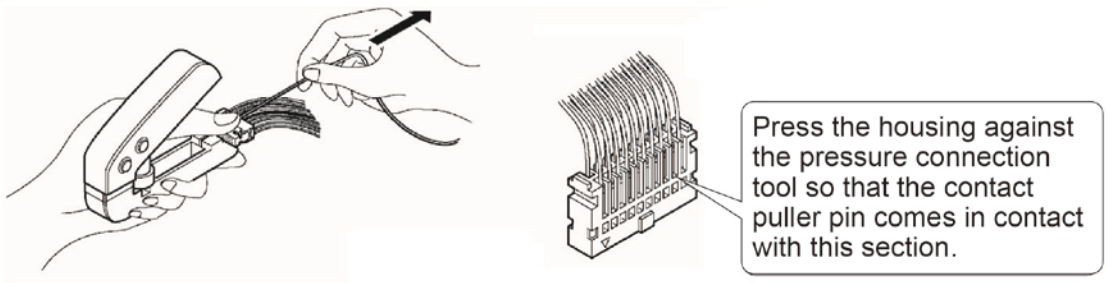


4. When all wires have been inserted, fit the semi-cover into place.



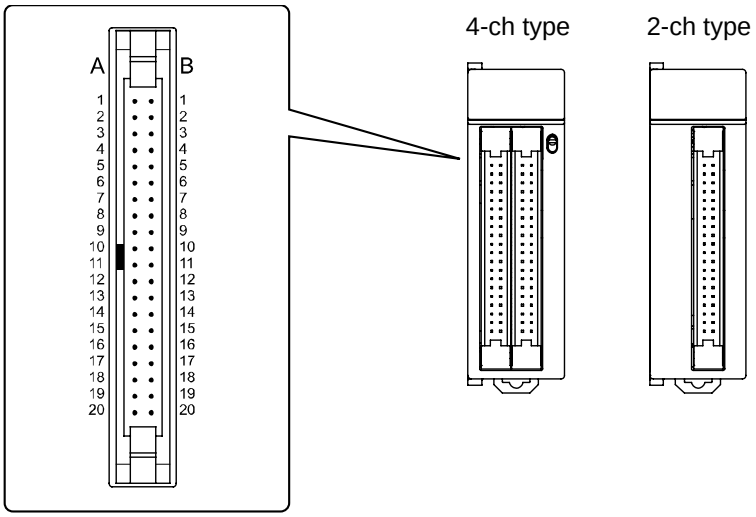
◆ KEY POINTS

- **Contact puller pin to redo wiring**
  If there is a wiring mistake or the wire is incorrectly pressure-connected, use the contact puller pin provided with the fitting to remove the contact.



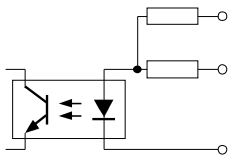
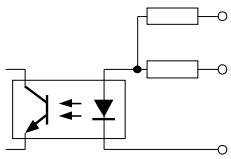
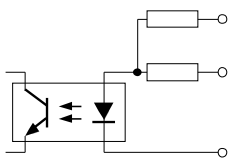
3.2 Terminal Circuit Diagram

3.2.1 I/O Terminal Layout Diagram

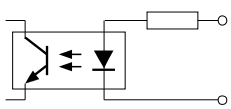
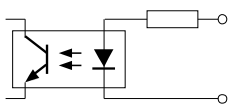


- Two connectors are used to connect the 4-ch type and one connector to connect the 2-ch type.
- The signal pins for two channels are assigned to one connector. There is no difference in pin arrangement between the CH0/CH1 connector and the CH2/CH3 connector if the unit is of the 4-ch type. Any pins with the same in number have the same function.

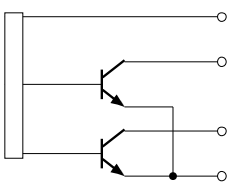
Input terminal

Pin No.		Circuit	Signal name
ch0/2	ch1/3		
A1	A11		Input A: 24 VDC (12 to 24 VDC)
A2	A12		Input A: 5 VDC (3.5 to 5 VDC)
B1	B11		Input A: COM
B2	B12		Input A: COM
A3	A13		Input B: 24 VDC (12 to 24 VDC)
A4	A14		Input B: 5 VDC (3.5 to 5 VDC)
B3	B13		Input B: COM
B4	B14		Input B: COM
A5	A15		Input Z: 24 VDC (12 to 24 VDC)
A6	A16		Input Z: 24 VDC (3.5 to 5 VDC)
B5	B15		Input Z: COM
B6	B16		Input Z: COM

Control 0/1 (common)

Pin No.		Circuit	Signal name
ch0/2	ch1/3		
A7	A17		Control 0: (12 to 24 VDC)
B7	B17		Control 0: COM
A8	A18		Control 1: (12 to 24 VDC)
B8	B18		Control 1: COM

External output 0/1 and Power supply terminal (common)

Pin No.		Circuit	Signal name
ch0/2	ch1/3		
A9	A19		External output 0: Sink output (5 to 24 VDC, 15 mA)
B9	B19		External output 1: Sink output (5 to 24 VDC, 15 mA)
A10	A20		Power supply for output: 24 VDC
B10	B20		Power supply for output: GND

(Note 1): For using external output (A9, A19, B9, B19), power should be supplied to the power supply for output (A10, A20, B10, B20). When the external output is not used, there is no need to supply the power to the power supply for output.

3.3 Input/Output Specifications

3.3.1 Input Specifications

Item	Description			
	Input A, B, Z signals			Control signal
	24VDC	5VDC		
		Open collector connection	Line driver connection	
Insulation method	Optical coupler			Optical coupler
Rated input voltage	12 V DC to 24 V DC	5VDC	Equivalent to AM26LS31	12VDC to 24VDC
Operating voltage range	10.8 V DC to 26.4 V DC	3.5VDC to 5.5VDC		10.8VDC to 26.4VDC
Input points per common	Independent common for each point			Independent common for each point
Min. on voltage/Min. on current	10V DC / 4 mA	3 V DC / 4 mA		10 V DC / 4 mA
Max. off voltage/Max. off current	2V DC / 2mA	1 V DC / 0.5 mA		2V DC / 2 mA
Input impedance	Approx. kΩ	Approx. 390 Ω		Approx. 3 kΩ
Operating mode indicator	LED display			LED display

(Note) The duty ratio of count input should be 50±10%. Also, the phase shifting of 2-phase input should be less than 5%.

3.3.2 Output Specifications

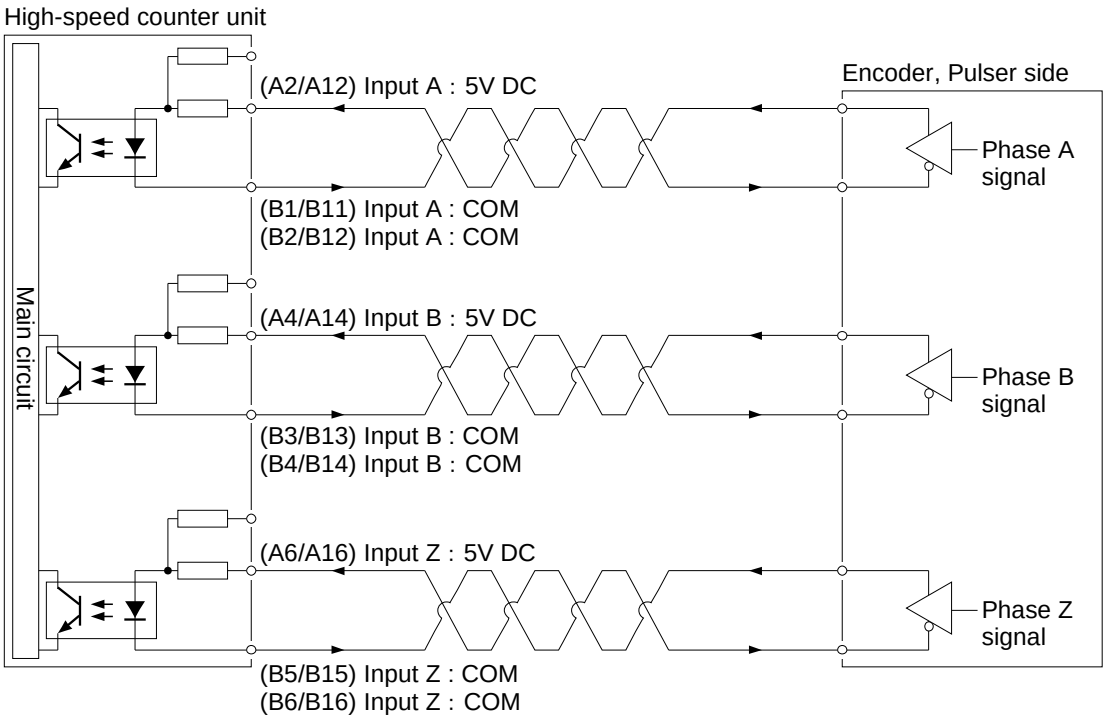
Item		Description
Insulation method		Optical coupler
Output type		Open collector (Sink output)
Rated load voltage		5 V DC to 24 V DC
Allowable load voltage range		4.75 V DC to 26.4 V DC
Max. load current		15 mA
Output points per common		2 points/common
Off state leakage current		1 μA or less
ON Max. voltage drop		0.2 VDC or less
External power supply	Voltage	21.6VDC to 26.4VDC
	Current	30 mA or less
Surge absorber		Zener diode
Operating mode indicator		LED display

3.4 Precautions on Wiring and Connection of Count Input

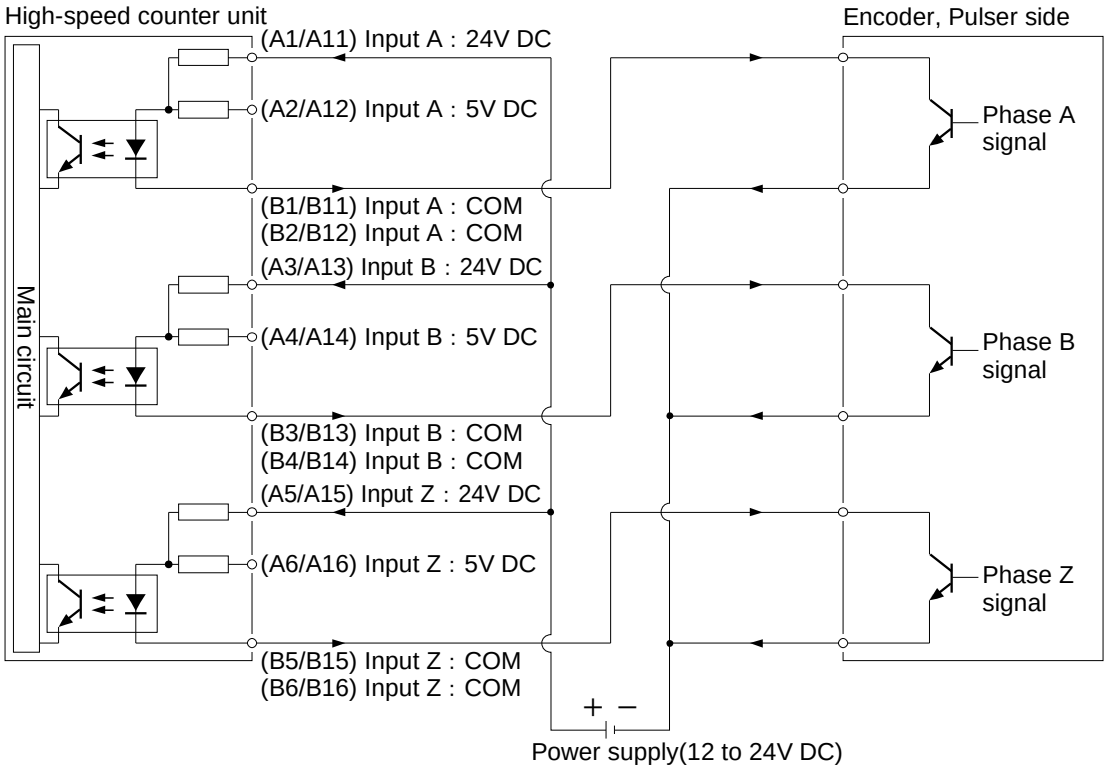
3.4.1 Precautions on Wiring

- For the connection between the count input (phases A, B, Z) and encoder, etc., use shielded twisted-pair cables.
- The length of connected wires should be within 10 m.

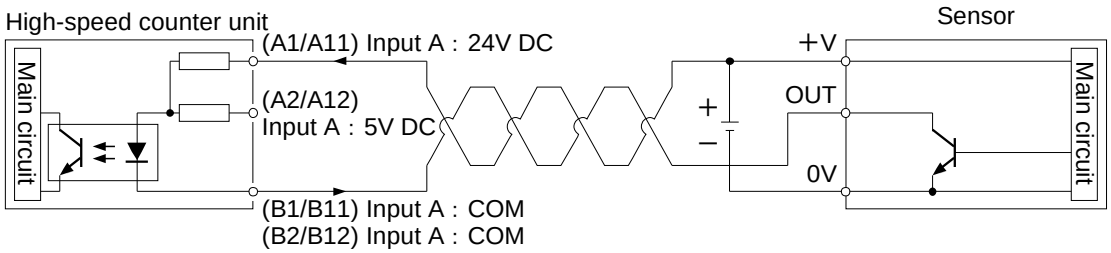
3.4.2 For Line Driver of Encoder Input



3.4.3 For Transistor Open Collector Type of Encoder Input



3.4.4 For Sensor Input



4

Unit Allocation and Parameter Settings

4.1 Unit Allocation

4.1.1 Confirmation of I/O Allocation Information

Input and output relays are allocated.

■ **Input relays**

I/O number								Name	Description
CH0		CH1		CH2		CH3			
WX0	X0	WX2	X20	WX4	X40	WX6	X60	Operation ready done	Flag to indicate the counter operation is ready.
	X1		X21		X41		X61	Counter enable	Flag to indicate the counter operation is enabled.
	X2		X22		X42		X62	Count direction	Flag to indicate a count direction. ON: Forward (Addition) OFF: Reverse (Subtraction)
	X3		X23		X43		X63	—	—
	X4		X24		X44		X64	Capture 0 done flag	Flag to announce that the count value is stored in capture 0 register.
	X5		X25		X45		X65	Capture 1 done flag	Flag to announce that the count value is stored in capture 1 register.
	X6		X26		X46		X66	External output 0 signal monitor	Monitors the output state of external output 0 signal.
	X7		X27		X47		X67	External output 1 signal monitor	Monitors the output state of external output 1 signal.
	X8		X28		X48		X68	Input A signal monitor	Monitors the input state of input A signal.
	X9		X29		X49		X69	Input B signal monitor	Monitors the input state of input B signal.
	XA		X2A		X4A		X6A	Input Z signal monitor	Monitors the input state of input Z signal.
	XB		X2B		X4B		X6B	Control 0 signal monitor	Monitors the output state of control 0 signal.
	XC		X2C		X4C		X6C	Control 1 signal monitor	Monitors the output state of control 1 signal.
	XD		X2D		X4D		X6D	Overflow annunciation	Flag to announce the occurrence of overflow or underflow (Enabled for the linear counter only.)
	XE		X2E		X4E		X6E	Underflow annunciation	
	XF		X2F		X4F		X6F	Error annunciation	Flag to announce the occurrence of an error.
WX1	X10 ~ X19	WX3	X30 ~ X39	WX5	X50 ~ X59	WX7	X70 ~ X79	Comparison match 0 flag ~ Comparison match 9 flag	Flag to reflect the results of the band comparison function or target value match function.
	X1A ~ X1F		X3A ~ X3F		X5A ~ X5F		X7A ~ X7F	Comparison match A flag ~ Comparison match F flag	

(Note 1): The I/O numbers actually allocated are the numbers based on the starting word number allocated to the unit.
Example) When the starting word number for the unit is "10", the operation ready done flag for CH0 is X100.

■ **Output relays**

I/O number								Name	Enabled condition	Description
CH0		CH1		CH2		CH3				
WY0	Y0	WY1	Y10	WY2	Y20	WY3	Y30	Operation ready request	Level	Relay to recalculate the setting parameter of counter.
	Y1		Y11		Y21		Y31	Count enable request	Level	Relay to start the counter operation.
	Y2		Y12		Y22		Y32	Reset request	ON edge	Relay to reset count values.
	Y3		Y13		Y23		Y33	Preset request	ON edge	Relay to preset count values.
	Y4		Y14		Y24		Y34	Reset enable request	Level	Relay to enable the reset by the control signal and input Z signal.
	Y5		Y15		Y25		Y35	Current value change request	ON edge	Relay to request for changing the current value of counter.
	Y6		Y16		Y26		Y36	Preset value change request	ON edge	Relay to request for changing preset values.
	Y7		Y17		Y27		Y37	Capture enable request (Note 2)	Level	Capture enable request when using the capture function or capture trigger signal when using the sampling capture function.
	Y8		Y18		Y28		Y38	—	—	—
	Y9		Y19		Y29		Y39	External output 0 forced ON	Level	Relay to forcibly turn on the external output 0.
	YA		Y1A		Y2A		Y3A	External output 0 forced OFF	Level	Relay to forcibly turn off the external output 0.
	YB		Y1B		Y2B		Y3B	External output 1 forced ON	Level	Relay to forcibly turn on the external output 1.
	YC		Y1C		Y2C		Y3C	External output 1 forced OFF	Level	Relay to forcibly turn off the external output 1.
	YD		Y1D		Y2D		Y3D	Overflow clear	ON edge	Relay to clear the overflow annunciation flag.
	YE		Y1E		Y2E		Y3E	Underflow clear	ON edge	Relay to clear the underflow annunciation flag.
	YF		Y1F		Y2F		Y3F	Error clear	ON edge	Relay to clear errors.

(Note 1): The I/O numbers actually allocated are the numbers based on the starting word number allocated to the unit.
Example) When the starting word number for the unit is "10", the operation ready request flag for CH0 is Y100.

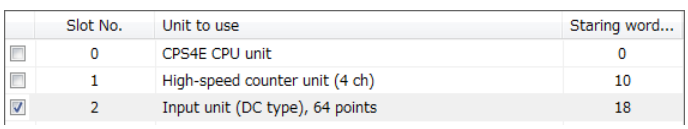
(Note 2) How the capture enable request signal works varies according to the functions to be used.

4.1.2 Number of Occupied Points of High-speed Counter Unit

- The following I/O numbers are used for the high-speed counter unit.
- As the input and output starts from the same I/O numbers in FP7 series, the following number of words is occupied.

Name	Product No.	No. of I/O points actually used		No. of occupied words (No. of occupied points)
		Input	Output	
2-ch type	AFP7HSC2T	8 words (128 points)	4 words (64 points)	8 words (128 points)
4-ch type	AFP7HSC4T			

Example) The both 2-ch type and 4-ch type high-speed counter units occupy 8 words (128 points).



	Slot No.	Unit to use	Staring word...
☐	0	CPS4E CPU unit	0
☐	1	High-speed counter unit (4 ch)	10
☑	2	Input unit (DC type), 64 points	18

4.1.3 Registration in I/O Map

Before setting parameters, register the unit to be used in the I/O map.

◆ **PROCEDURE**

1. **Select "Options" > "FP7 Configuration" in the menu bar.**

   The FP7 Configuration dialog box is displayed.

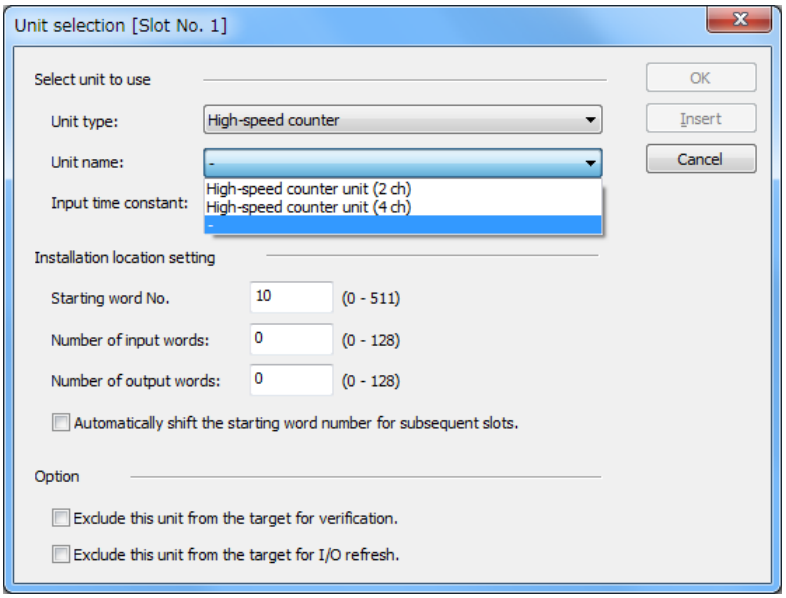
2. **Select "I/O map" in the left pane.**

   The allocation menu of the I/O map is displayed.

3. **Double-click a desired slot.**

   The Unit selection dialog box is displayed.

4. **Select "High-speed counter" for "Unit type" and select the unit name used, and press the "OK" button.**



The selected unit is now registered in the I/O map.

4.2 Configuration of High-speed Counter Unit

4.2.1 Configuration Using Tool Software

The counter type, operation mode and the settings of the high-speed counter are specified in the configuration menu of FPWIN GR7.

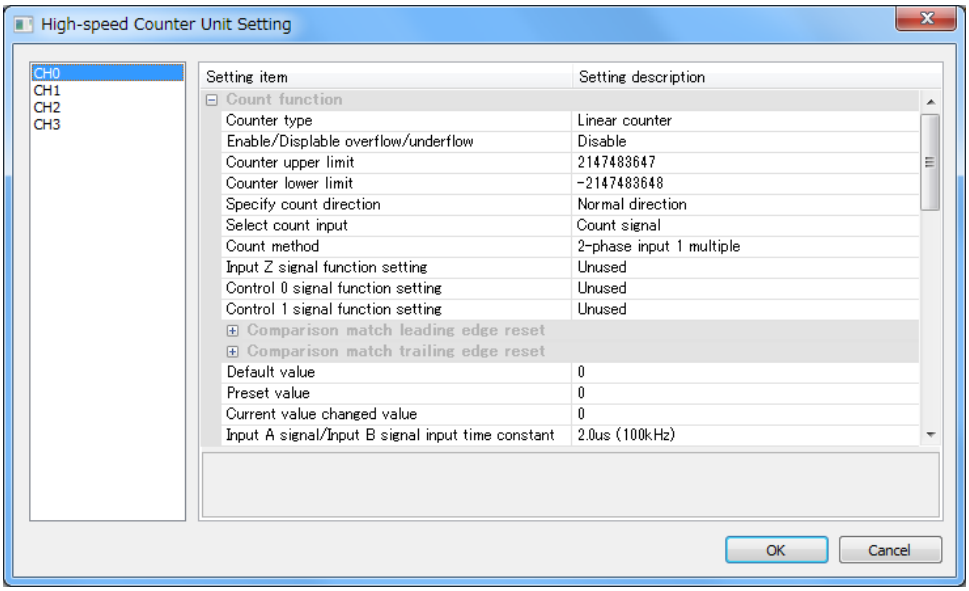
■ **Setting method**

The following procedure describes the process when the high-speed counter unit has been already allocated in the I/O map.

◆ **PROCEDURE**

1. **Select "Options" > "FP7 Configuration" in the menu bar.**
2. **Select "I/O map" in the field.**
3. **Select the slot where the high-speed counter unit has been registered, and select the "Advanced" button.**

   The High-speed Counter Unit Setting dialog box is displayed.



4. **Select items according to the conditions used.**
5. **Press the [OK] button.**
6. **The set values are downloaded with programs as a project, and will be effective when the operation ready request is executed.**

4.2.2 Configuration Data Setting Items

■ **Count function (Settable for each channel)**

item	Description	Default
Counter type	Linear counter/Ring counter	Linear counter
Enable/Disable overflow/underflow	Disable/Enable	Disable
Counter upper limit	-2,147,483,647 to 2,147,483,647	2,147,483,647
Counter lower limit	-2,147,483,648 to 2,147,483,646	-2,147,483,648
Count direction	Normal direction/Reverse direction	Normal direction
Count input selection	Count signal Internal clock 0.25 us (4 MHz) Internal clock 1.00 us (1 MHz) Internal clock 10 us (100 kHz) Internal clock 100 us (10 kHz)	Count signal
Count method	2-phase input 1 multiple, 2-phase input 2 multiple, 2-phase input 4 multiple, Individual input 1 multiple, Individual input 2 multiple, Direction detection input 1 multiple, Direction detection input 2 multiple	2-phase input 1 multiple
Input Z signal function setting	Not used Reset operation at rising edge Reset operation at trailing edge Positive logic reset operation Negative logic reset operation Preset operation at rising edge Preset operation at trailing edge Positive logic preset operation Negative logic preset operation	Not used
Control 0 signal function setting	Not used Positive logic enable operation Negative logic enable operation Positive logic enable operation and reset operation at rising edge Negative logic enable operation and reset operation at trailing edge Positive logic enable operation and preset operation at rising edge Negative logic enable operation and preset operation at trailing edge	Not used
Control 1 signal function setting	Not used Positive logic enable operation Negative logic enable operation	Not used
Comparison match leading edge reset	Specify the comparison match flag used as a reset signal for resetting count values at the rising edge of comparison match flag.	Not reset
Comparison match trailing edge reset	Specify the comparison match flag used as a reset signal for resetting count values at the trailing edge of comparison match flag.	Not reset
Default value	Set the count value when the power is turned on. -2,147,483,648 to 2,147,483,647	0
Preset value	Set the count value for the preset operation. -2,147,483,648 to 2,147,483,647	0
Current value changed value	Set the current value changed value to change the count value. -2,147,483,648 to 2,147,483,647	0

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Input A signal/Input B signal input time constant Input Z signal input time constant	No input time constant, 0.1 us (2 MHz), 0.2 us (1 MHz), 0.5 us (500 kHz), 1.0 us (250 kHz), 2.0 us (100 kHz), 10.0 us (10 kHz)	2.0 us (100 kHz)
Control signal input time constant	No input time constant /2 us / 5 us / 10 us / 20 us / 50 us / 100 us / 500 us / 1.0 ms / 2.0 ms / 5.0 ms / 10.0 ms	2.0 ms

(Note 1): The control 0 signal and control 1 signal cannot be assinged to the capture function if they are assigned to the enable operation.

■ Measurement function (Settable for each channel)

item	Description	Default
Measurement function selection	Not use measurement function Frequency measurement Frequency measurement and rotation speed measurement A Frequency measurement and rotation speed measurement B	Not use measurement function
Pulse number per rotation	Set the pulse number for one rotation of the encoder. Setting range: 1 to 1,048,575	1
Average number of frequency measurement processes	No averaging, 2, 4, 8, 16, 32, 64, 128 times	No averaging
Average number of rotation speed measurement processes	No averaging, 2, 4, 8, 16, 32, 64, 128 times	No averaging

■ Comparison function (Settable for each channel)

item	Description		Default
Comparison function selection	Not use Band comparison Target value match comparison		Not use
Comparison input selection	Count value Measurement value (Frequency) Measurement value (Rotation speed)		Count value
Nmber of comparison data	Set the judgement value for the comparison function. Setting range: 1 to 16		16
Comparison data 0 ~ Comparison data 15 (For band comparison)	Specify the lower and upper limits for each comparison data. (Note 1) Setting range: -2,147,483,648 to 2,147,483,647		0
	Select the set patterns, on or off, for the comparison match 0 flag to the comparison match F flag for each comparison data.		OFF
Comparison data 0 ~ Comparison data 15 (For target value match)	Specify target values for each comparison data. Setting range: -2,147,483,648 to 2,147,483,647		0
	Select the pattern, set or reset, according to the situation when reaching the target value (addition or subtraction) for each comparison data.		No change
	Addition set pattern:	Set output, no change	
	Addition reset pattern:	Reset output, no change	
	Subtraction set pattern:	Set output, no change	
	Subtraction reset pattern:	Reset output, no change	

(Note 1): Lower and upper limits can be set in the range of the lower and upper limits of the counters.
For the linear counter, the set lower limit should be less than the upper limit. For the ring counter, they can be set in any range.

■ External output function (Settable for each channel)

item		Description	Default
External output 0	Signal setting	Not output/Output	Not output
	Output hold setting	Set the condition of the output when a CPU or high-speed counter error occurs. Not hold/Hold	Not hold
	ON timing delay	Setting range: 0 to 1,000 ms	0 ms
	ON hold time	Setting range: 0 to 1,000 ms	0 ms
External output 1	Signal setting	Not output/Output	Not output
	Output hold setting	Set the condition of the output when a CPU or high-speed counter error occurs. Not hold/Hold	Not hold
	ON timing delay	Setting range: 0 to 1,000 ms	0 ms
	ON hold time	Setting range: 0 to 1,000 ms	0 ms

(Note 1): The ON timing delay and ON hold time are enabled only when the band comparison function is used.

■ Capture function (Settable for each channel)

item	Description	Default
Capture 0 setting	Not use capture 0 function Capture function at rising edge of control 0 signal Capture function at trailing edge of control 0 signal Capture function at rising edge of control 1 signal Capture function at trailing edge of control 1 signal Control 0 signal positive logic sampling capture function Control 0 signal negative logic sampling capture function Control 1 signal positive logic sampling capture function Control 1 signal negative logic sampling capture function Output relay (Y relay) sampling capture function	Not use
Capture 1 setting	Not use capture 1 function Capture function at rising edge of control 0 signal Capture function at trailing edge of control 0 signal Capture function at rising edge of control 1 signal Capture function at trailing edge of control 1 signal	Not use
Sampling capture function operation setting	One operation/Continuous operation	One operation
Sampling time	1 to 65,535 ms	1ms

(Note 1): When the sampling capture function has been selected in the capture 0 setting, the capture 1 setting is invalid.

■ Interrupt function (Settable for each channel)

item	Description		Default
Interrupt function enable/disable setting	Comparison match 0 flag	Enable/Disable	Enable
	Comparison match 1 flag	Enable/Disable	Enable

(Note 1): Use the dip switches on the side of the unit to enable the interrupt function.

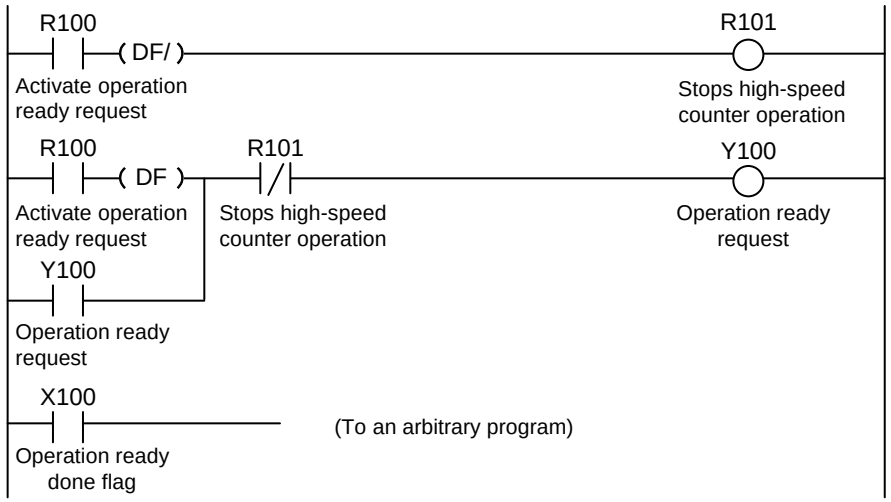
4.3 Configuration Data and Operation Ready Request

4.3.1 Operation Ready Request Program

- For enabling the settings of the high-speed counter unit, the operation ready request program should be executed.
- After downloading a project, insert the program to make it be executed early in the process.

■ Operation ready request program

Example) Program to request the preparation of the CH0 operation of the high-speed counter unit installed in the slot 1



■ Allocation of I/O signals

Signal name	Effective condition	CH0	CH1	CH2	CH3
Operation ready request	Level	Y100	Y110	Y120	Y130
Operation ready done flag	-	X100	X120	X140	X160

(Note 1): The above I/O numbers are those for the slot number 1 and the starting word number 10. The I/O numbers actually used vary according to the slot number where the unit is installed and the starting word number.

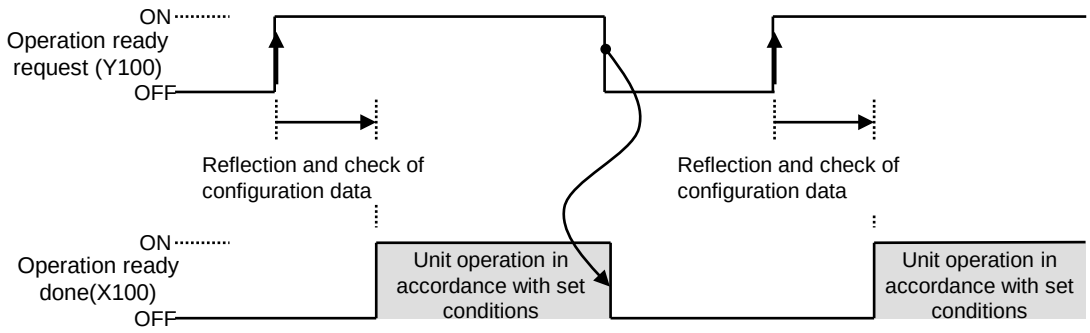
4.3.2 Downloading Configuration Data

- The configuration information of the high-speed counter unit is downloaded to the CPU together with user programs.
- The above programs are executed in the RUN mode, and each function of the high-speed counter unit will be enabled once the operation ready done flag turns on.

4.3.3 Operation When Operation Ready Request Program is Executed

- The operation ready done flag will be on when the operation ready request program is executed and each operation set in the unit becomes executable.

■ **Operation of operation ready request flag**



◆ **KEY POINTS**

- **When an error occurs, such as an abnormality in the settings of parameters, the operation ready done flag will not be turned on.**

4.4 Configuration Using User Programs

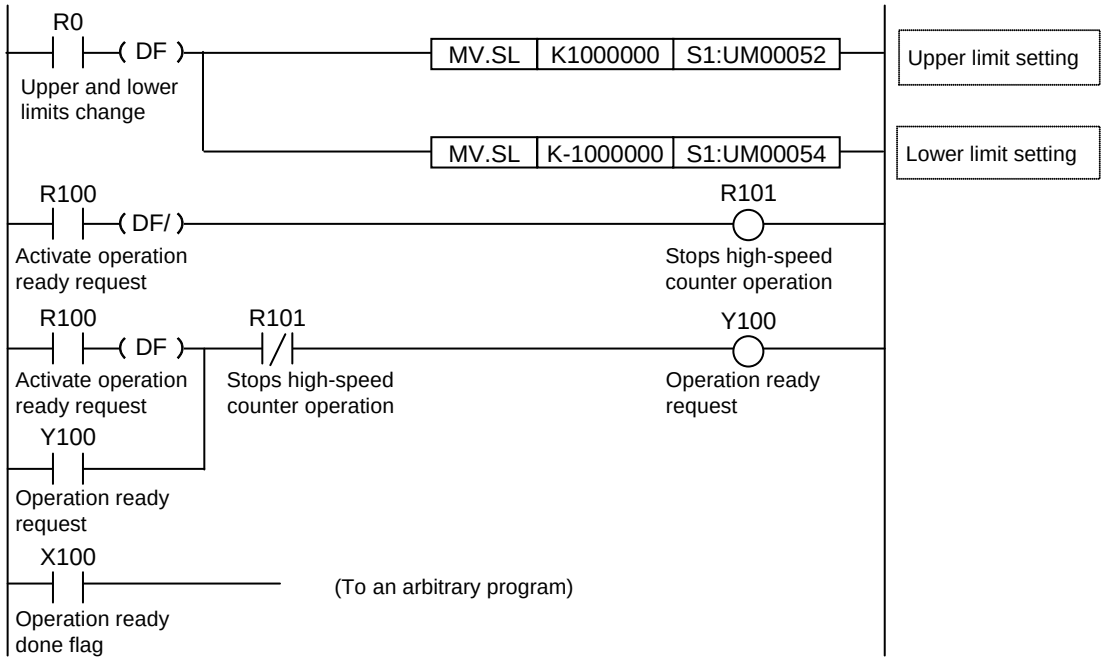
Configuration information can be rewritten using user programs.

■ Overview of function

- The values of configuration information are stored in unit memories (UM) in which arbitrary parameters are set. The values will be updated by turning on the operation ready request flag (Y0) when you want to reflect them in the configuration.
- If the configuration information is updated, the operation ready done flag (X0) will be on.

■ Sample program

Program to change the upper and lower limits of CH0 of the high-speed counter unit installed in the slot 1 using user programs



■ Allocation of I/O signals

Signal name	Effective condition	CH0	CH1	CH2	CH3
Operation ready request	Level	Y100	Y110	Y120	Y130
Operation ready done flag	-	X100	X120	X140	X160

(Note 1): The above I/O numbers are those for the slot number 1 and the starting word number 10. The I/O numbers actually used vary according to the slot number where the unit is installed and the starting word number.

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◆ KEY POINTS

- **The configuration using user programs can be changed even when the counter is running. However, the changed values will not be effective until the operation ready done flag (X0) is turned on.**
- **The operation ready request can be executed for each channel regardless whether it has been executed in other channels or not.**

5
Count Function

5.1 Selection of Counters and Basic Settings

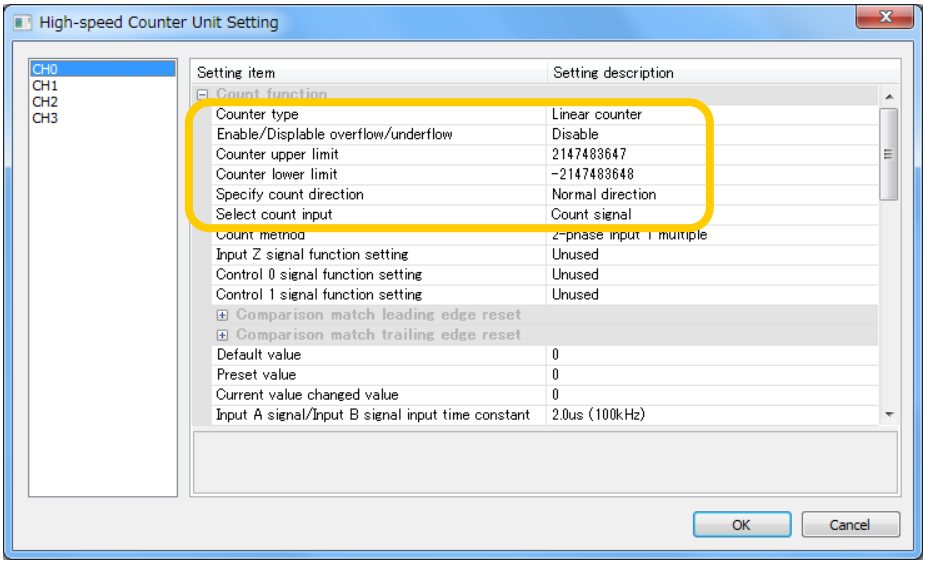
5.1.1 Basic Settings of Counters

The basic settings are set in the configuration menu of FPWIN GR7 or unit memories (UM).

■ **Count function configuration**

Item	Description	Default
Counter type	Linear counter/Ring counter	Linear counter
Enable/Disable overflow/underflow	Disable/Enable	Disable
Counter upper limit	-2,147,483,647 to 2,147,483,647	2,147,483,647
Counter lower limit	-2,147,483,648 to 2,147,483,646	-2,147,483,648
Specify count direction	Normal direction/Reverse direction	Normal direction
Select count input	Count signal / Internal clock 0.25 us (4 MHz) / Internal clock 1.00 us (1 MHz) / Internal clock 10us (100 kHz) / Internal clock 100 us (10 kHz)	Count signal
Count method	2-phase input 1 multiple, 2-phase input 2 multiple, 2-phase input 4 multiple, Individual input 1 multiple, Individual input 2 multiple, Direction detection input 1 multiple, Direction detection input 2 multiple	2-phase input 1 multiple

■ **Example of settings by FPWIN GR7**



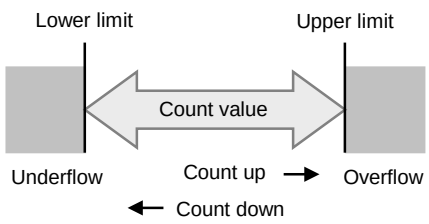
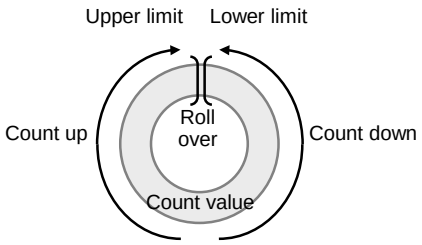
5.1.2 Selection of Count Input

- Select the count input to import input signals from an external device.
- For measuring the frequencies of external input signals or time based on the internal clock of the unit, select "Internal clock".

5.1.3 Linear Counter and Ring Counter

The operation changes depending on the types of counter as below.

■ **Operational difference between the counter types**

Comparison item	Linear counter	Ring counter
Operation image		
Operation when reaching the upper limit or lower limit	If the count value exceeds the upper limit, the upper limit will be held. If the count value falls below the lower limit, the lower limit will be held. (Note 1) (Note 2)	If the count value exceeds the upper limit, the count value will be the lower limit automatically and the count operation will continue. If the count value falls below the lower limit, the count value will return to the upper limit automatically and the count operation will continue. (Note 1)
Overflow and underflow settings	It can be announced as an error by the setting of configuration menu. If the lower limit or the upper limit has been set using the configuration menu, an error is announced based on the set values.	Not settable.

(Note 1): When the upper limit or the lower limit has been changed in the configuration menu, the counter operates based on its range.

(Note 2): Even when the upper and lower limits have been set on the linear counter, counting continues up to the range that is countable as a system (-2,147,483,648 to 2,147,483,647) if the overflow and under flow settings have been set to "Disable".

■ **Operation in case of overflow or underflow (Linear counter only)**

- When "Enable" has been selected in the configuration menu, the error will be announced once the overflow or underflow annunciation flag turns on.
- The overflow or underflow flag can be cleared by the following operations; Overflow clear request, Underflow clear request, Reset or Preset operation
- The error clear operation is required to clear error flags.

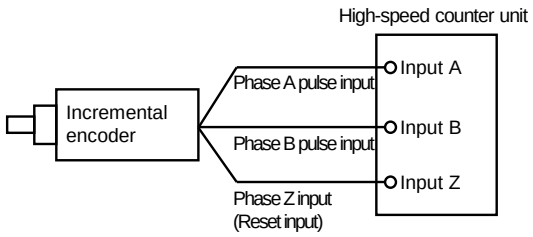
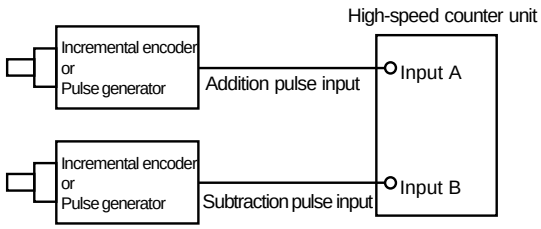
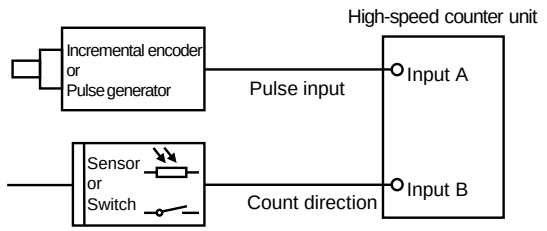
◆ **REFERENCE**

- **For details of the error clear method, refer to 10.1 Self-diagnostic Function.**

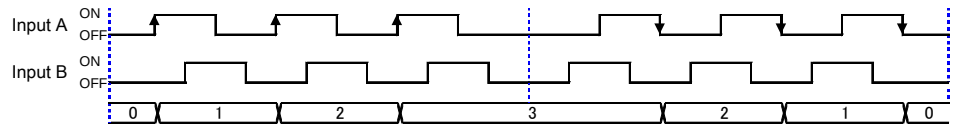
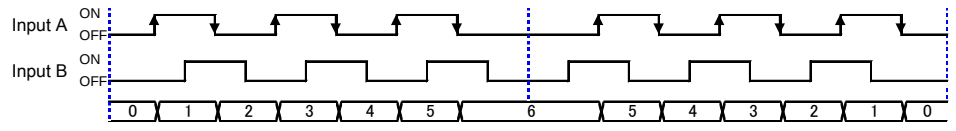
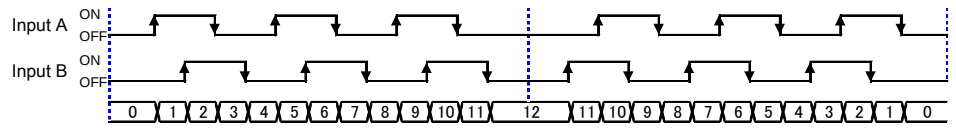
5.1.4 Selection of Count Methods

- Select from the following three types according to input devices to be connected.
- The count operation varies depending on the settings of multiplication factor as shown in the next page.

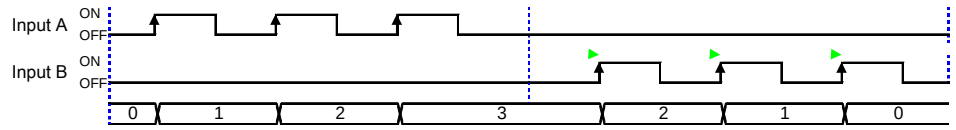
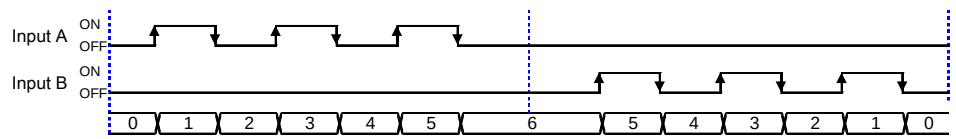
■ **Count method**

Method	Connection	Count
2-phase (Phase difference)		For the 2-phase input, the input A signal and input B signal of each counter are connected to the phase A and phase B of an encoder. The count direction depends on the phase difference between phases A and B. When the phase A is proceeding by 90 degrees in electrical angle than the phase B, the count value is incremented. When the phase A is delayed by 90 degrees in electrical angle than the phase B, the count value is decremented.
Individual		In the individual input method, the counter is incremented when the input A signal rises or falls, and decremented when the input B signal rises or falls.
Direction detection		For the direction detection input, the count signal is connected to the input A signal. The count direction is controlled by the level of the direction signal of input B signal. When the input B signal is on, the counter is incremented when the input A signal rises or falls. When the input B signal is off, the counter is decremented.

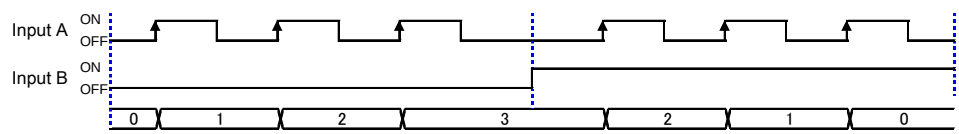
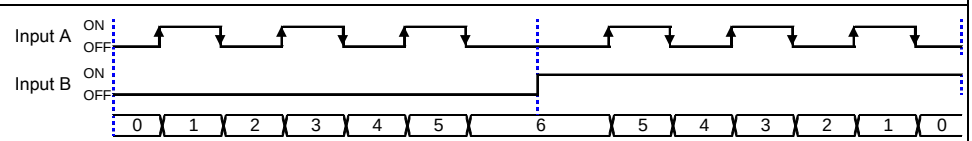
■ Count operation of 2-phase input (Phase difference input)

Multiplication factor	Time chart	
	Addition	Subtraction
1 multiple		
2 multiple		
4 multiple		

■ Count operation of individual input

Multiplication factor	Time chart	
	Addition	Subtraction
1 multiple		
2 multiple		

■ Count operation of direction detection input

Multiplication factor	Time chart	
	Addition	Subtraction
1 multiple		
2 multiple		

5.2 Types of Count Operations

5.2.1 Types and Features of Count Operations

■ Types of count operations and input signals

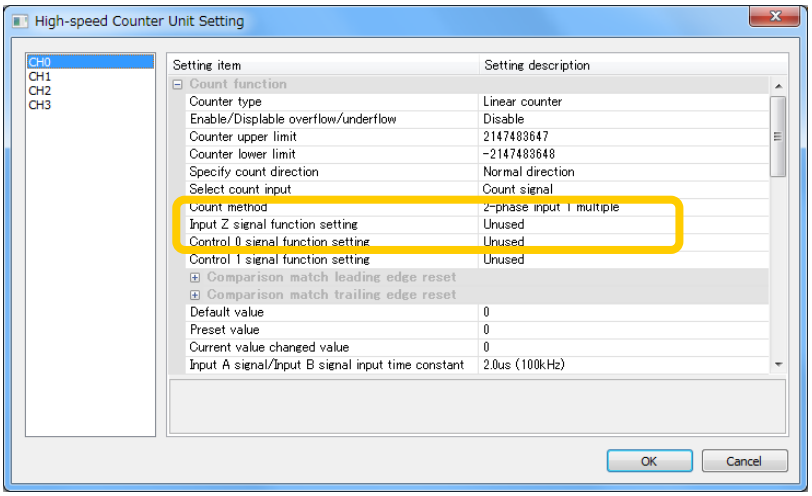
Operation Type	Feature	External input signal used		
		Z-phase input signal	Control 0 signal	Control 1 signal
Simple count operation	Performs the count operation regardless of external control input signals.			
Reset count operation	Performs the reset operation according to the change in the z-phase input signal (rising, trailing, positive logic or negative logic).	●		
Preset count operation	Performs the preset operation according to the change in the z-phase input signal (rising, trailing, positive logic or negative logic).	●		
Enable count operation	Performs the count operation while the control signal allocated to the enable input is effective.		●	●
Enable reset count operation	Performs the count operation while the control signal allocated to the enable input is effective. Resets the count value at the timing at which the counter becomes enabled by the control signal allocated to the enable input.		●	
Enable preset count operation	Performs the count operation while the control signal allocated to the enable input is effective. Presets the count value at the timing at which the counter becomes enabled by the control signal allocated to the enable input.		●	

(Note 1): In any of these cases, resetting or presetting values can be performed by output relays (Y).

(Note 2): If the control signals are used in the above operations, the same signals cannot be used for the capture function or sampling chapture function.

(Note 3) To enable the count input when selecting the simple count operation, reset count operation or preset count operation, it is necessary to turn on the count enable request signal (Y1) in user programs.

■ Example of settings by FPWIN GR7

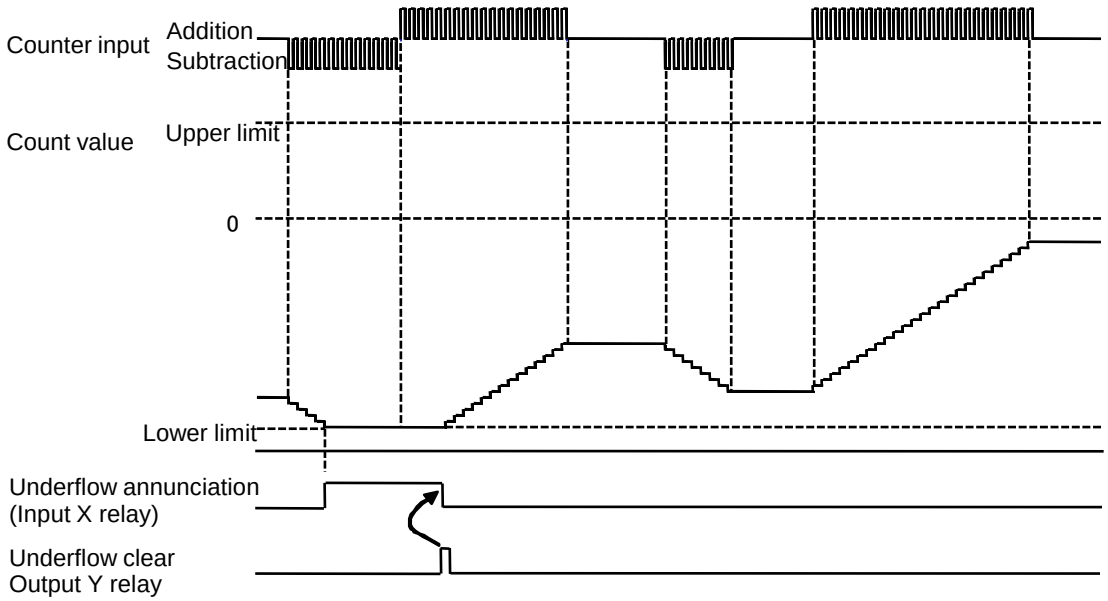


5.2.2 Simple Count Operation

- Simply counts count input signals.
- To enable the count input, it is necessary to turn on the count enable request signal (Y1) in user programs.

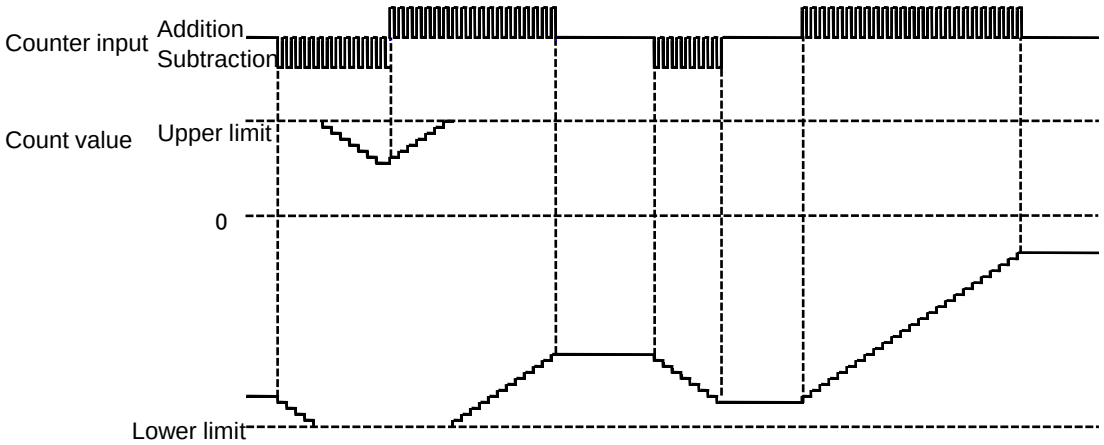
■ Linear counter

The overflow and underflow annunciation can be set for the cases when the count value exceeds the upper limit or the lower limit.



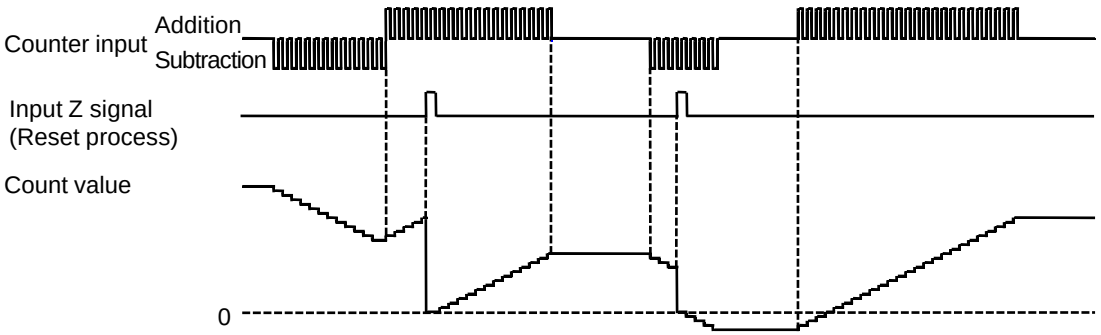
■ Ring counter

- If the lower limit is counted down, the count value will be rolled over, and counting down will continue from the upper limit.
- If the upper limit is counted up, the count value will be rolled over, and counting up will continue from the lower limit.


Counter input
Addition
Subtraction
Count value
Upper limit
0
Lower limit

5.2.3 Reset Count Operation

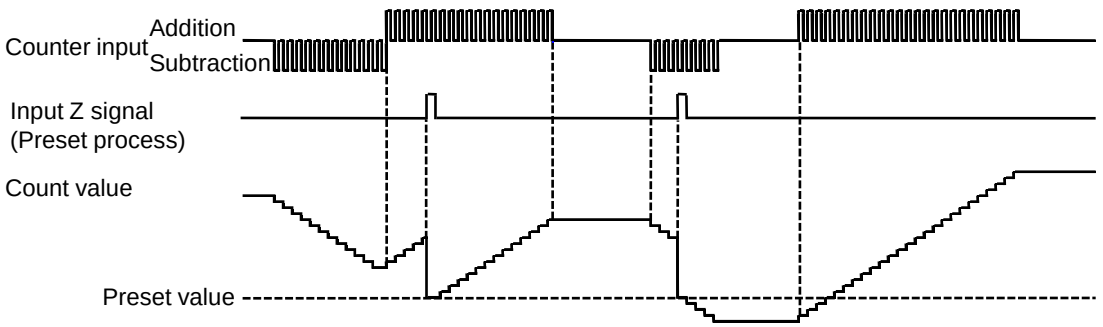
- Resets the count value to zero by the input Z signal.
- To enable the count input, it is necessary to turn on the count enable request signal (Y1) in user programs.



-

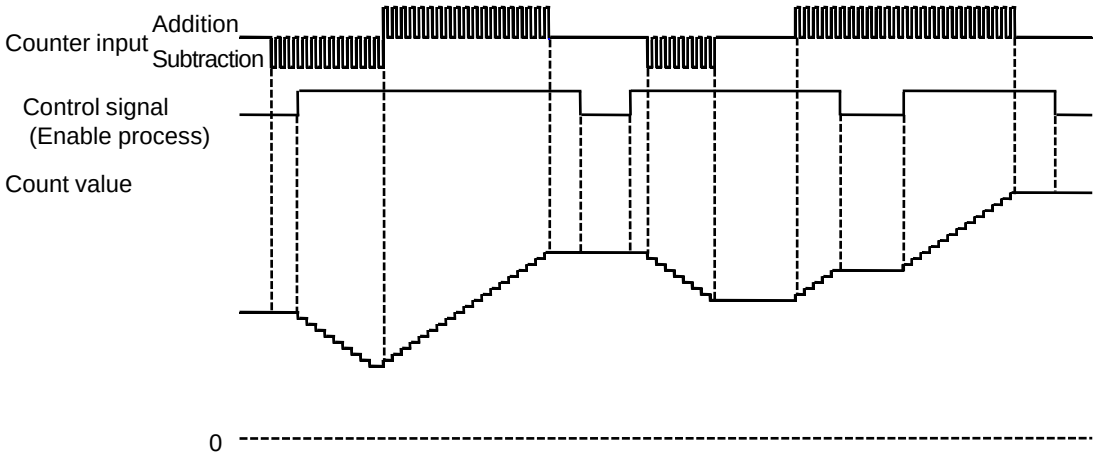
5.2.4 Preset Count Operation

- The preset count operation is allocated to the input Z signal and is used to change the current value of the counter to the preset value.
- To enable the count input, it is necessary to turn on the count enable request signal (Y1) in user programs.
- It can be also used for starting the counter operation from the preset value.
- The preset value is set in the configuration menu or unit memory (UM) area.



5.2.5 Enable Count Operation

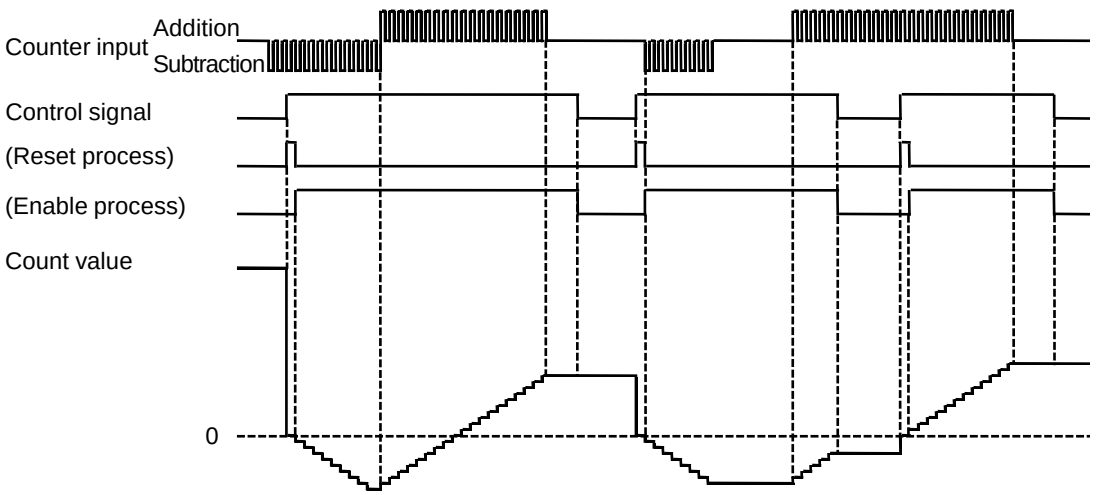
- The enable function is allocated to the control signal for using the enable count operation.
- Performs the count operation while the control signal is effective.



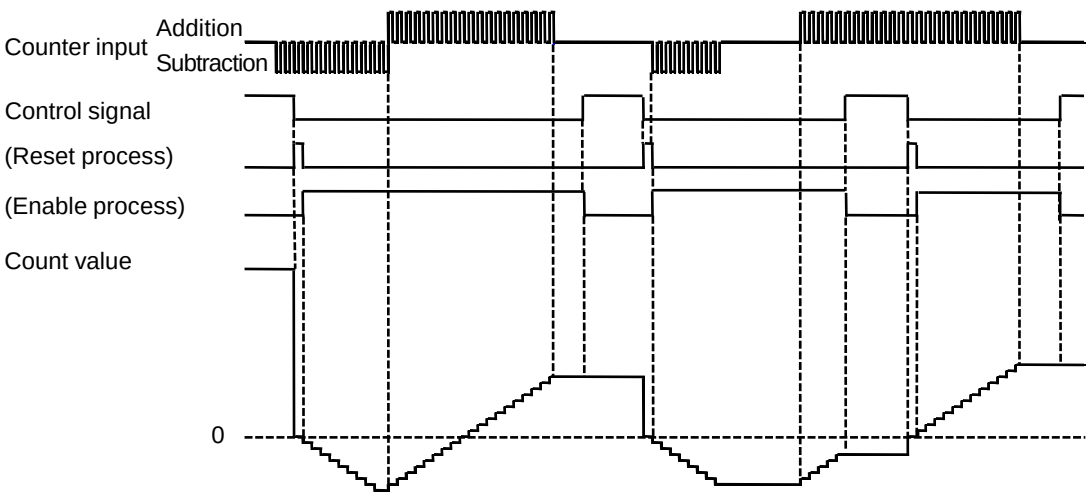
5.2.6 Enable Reset Count Operation

- The enable reset count operation is the operation that the enable and reset functions are allocated to the control signal.
- Resets the count value to zero when the counter becomes enabled by the change in the control signal.

■ **Positive logic enable operation and reset operation at rising edge**



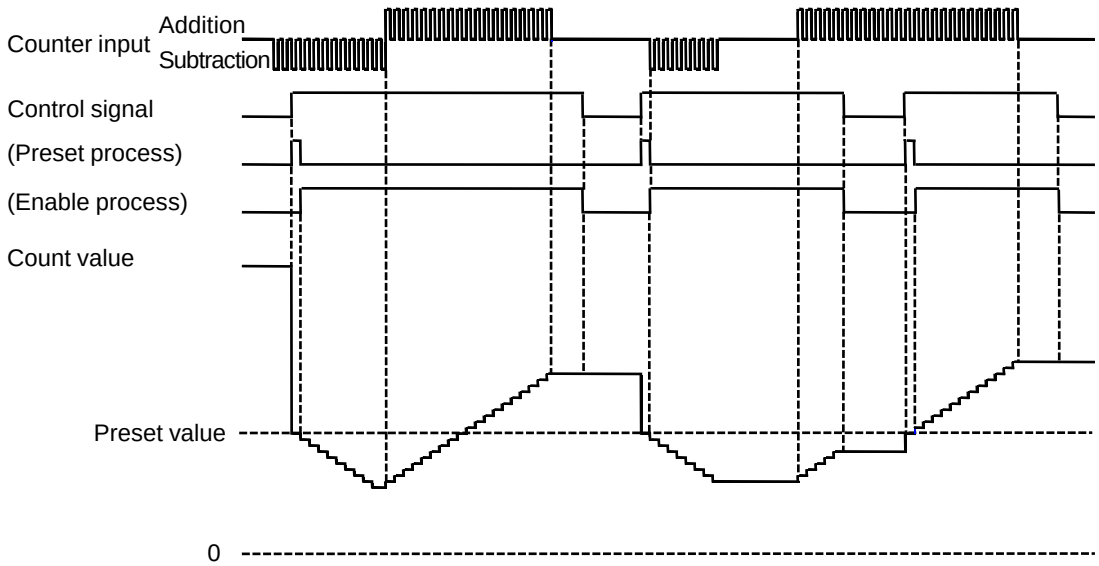
■ **Negative logic enable operation and reset operation at trailing edge**



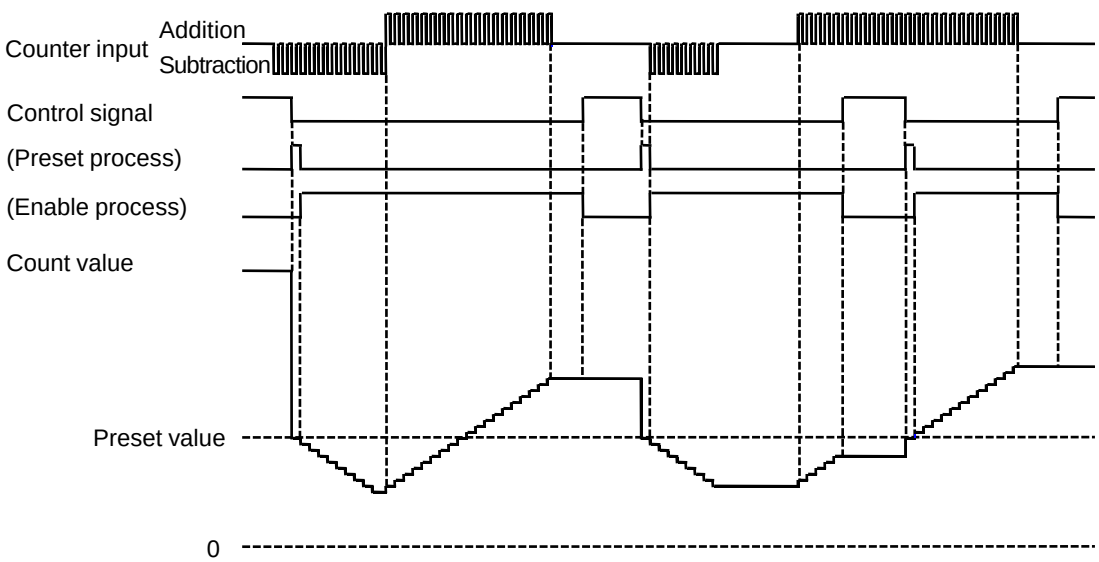
5.2.7 Enable Preset Count Operation

- The enable preset count operation is that the enable and preset functions are allocated to the control signal.
- Resets the count value to a specified preset value when the counter becomes enabled by the change in the control signal.

■ **Positive logic enable operation and preset operation at rising edge**



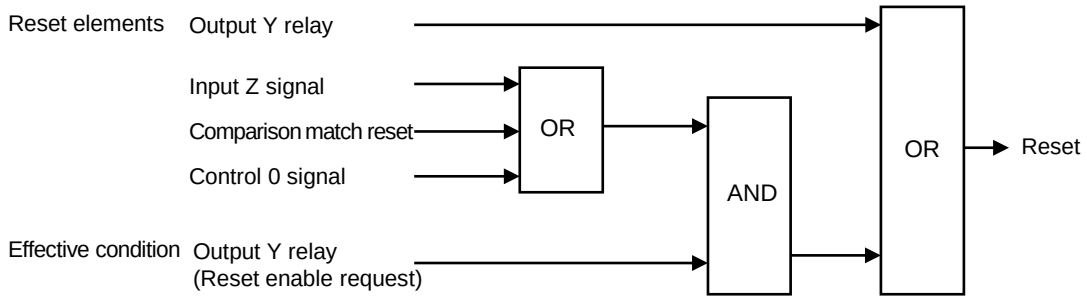
■ **Negative logic enable operation and preset operation at trailing edge**



5.3 Allocation of Reset, Preset and Enable Signals

5.3.1 Reset Input

The following four reset methods are available.



■ **Type of reset signals**

Reset element	Setting method	Reset condition			
		ON ····· OFF	ON OFF ·····	ON ··· OFF	ON OFF ···
Output Y relay	Activates the reset request signal by a user program.	●			
Input Z signal	Allocates the Z-phase input signal to any reset operation using the configuration menu.	●	●	●	●
Control 0 signal	Allocates the control 0 signal to either reset operation using the configuration menu. Positive logic enable operation and reset operation at rising edge Negative logic enable operation and reset operation at trailing edge	●	●		
Comparison match flag	Allocates the comparison match flag operation to "Reset execution" using the configuration menu.	●	●		

■ **I/O allocation**

Signal name	Effective condition	CH0	CH1	CH2	CH3
Reset request	ON edge	Y102	Y112	Y122	Y132
Reset enable request	Level	Y104	Y114	Y124	Y134
Input Z signal monitor	-	X10A	X12A	X14A	X16A
Control 0 signal monitor	-	X10B	X12B	X14B	X16B
Comparison match flag	-	X110-X11F	X130-X13F	X150-X15F	X170-X17F

(Note 1): The above I/O numbers are those for the slot number 1 and the starting word number 10. The I/O numbers actually used vary according to the slot number where the unit is installed and the starting word number.

◆ KEY POINTS

- **For using the Z-phase signal, control signal or comparison match flag as reset signals, turn on the reset enable request signal using user programs.**

5.3.2 Preset Input

The following three preset methods are available.

■ **Type of reset signals**

Preset element	Setting method	Preset condition			
		ON ····· OFF ┐└	ON ┐└ OFF ·····	ON ·· OFF ┐└	ON ┐└ OFF ··
Output Y relay	Activates the preset request signal by a user program.	●			
Input Z signal	Allocates the Z-phase input signal to either preset operation using the configuration menu.	●	●	●	●
Control 0 signal	Allocates the control 0 signal to either reset operation using the configuration menu. Positive logic enable operation and preset operation at rising edge Negative logic enable operation and preset operation at trailing edge	●	●		

■ **I/O Allocation**

Signal name	Effective condition	CH0	CH1	CH2	CH3
Preset request	ON edge	Y103	Y113	Y123	Y133
Input Z signal monitor	-	X10A	X12A	X14A	X16A
Control 0 signal monitor	-	X10B	X12B	X14B	X16B

(Note 1): The above I/O numbers are those for the slot number 1 and the starting word number 10. The I/O numbers actually used vary according to the slot number where the unit is installed and the starting word number.

■ **Setting of preset values**

Unit memory No. (Hex)	Name	Default	Setting range and description	Unit
UM 00062 UM 00063 UM 00132 UM 00133 UM 00202 UM 00203 UM 002D2 UM 002D3	Preset value	0	Set preset values. Setting range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse

◆ KEY POINTS

- **Preset values are set in unit memories (UM) using the configuration menu or user programs.**

5.3.3 Enable Input

The following enable input methods are available.

■ **Type of enable signals**

Enable operation element	Setting method	Enable condition	
			
Output Y relay	Activates the enable request signal by a user program.	●	
Control 0 signal	Allocates the control 0 signal to any of these operations using the configuration menu. Positive logic enable operation Negative logic enable operation Positive logic enable operation and reset operation at rising edge Negative logic enable operation and reset operation at trailing edge Positive logic enable operation and preset operation at rising edge Negative logic enable operation and preset operation at trailing edge	●	●
Control 1 signal	Allocates the control 1 signal to either operation using the configuration menu. Positive logic enable operation Negative logic enable operation	●	●

■ **I/O Allocation**

Signal name	Effective condition	CH0	CH1	CH2	CH3
Enable request	Level	Y101	Y111	Y121	Y131
Control 0 signal monitor	-	X10B	X12B	X14B	X16B
Control 1 signal monitor	-	X10C	X12C	X14C	X16C

(Note 1): The above I/O numbers are those for the slot number 1 and the starting word number 10. The I/O numbers actually used vary according to the slot number where the unit is installed and the starting word number.

◆ **KEY POINTS**

- **The enable input works as a level signal.**

5.4 Reading Count Value and Changing Current Value

5.4.1 Areas Related to Count Value

■ **Monitor area related to count values**

Unit memory No. (Hex)	Name	Default	Setting range and description	Unit
UM 003A0 UM 003A1	Count value Current value	0	Current count value of counter Setting range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
UM 003B0 UM 003B1				
UM 003C0 UM 003C1				
UM 003D0 UM 003D1				

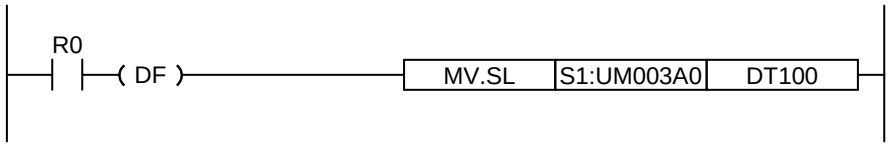
■ **Configuration area related to count value**

Unit memory No. (Hex)	Name	Default	Setting range and description	Unit
UM 00060 UM 00061	Default value (when power turns on)	0	Set the default value used when the power turns on. Setting range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
UM 00130 UM 00131				
UM 00200 UM 00201				
UM 002D0 UM 002D1				
UM 00062 UM 00063	Preset value	0	Set the preset value for using the preset count function. Setting range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
UM 00132 UM 00133				
UM 00202 UM 00203				
UM 002D2 UM 002D3				
UM 00064 UM 00065	Current value changed value	0	Set the changed value to change the current value of counter. Setting range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
UM 00134 UM 00135				
UM 00204 UM 00205				
UM 002D4 UM 002D5				

5.4.2 Reading Count Value

- The count value (current value) can be read from the monitor area.

Example) Program to change the current value of CH0 of the high-speed counter unit



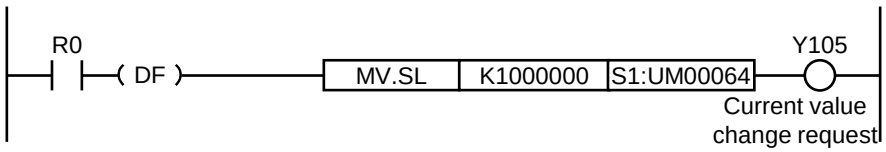
5.4.3 Count Value When Power Turns On

- The count value when the power turns on can be set to any value as necessary. Set the default value (when the power turns on) using the configuration menu of tool software FPWIN GR7 or user programs.
- The default for the count value when the power turns on is "0".

5.4.4 Changing Count Current Value

- The count current value can be set to any value as necessary.
- Set a value in the current value changed value area using the user program and turn on the current value change request signal.

Example) Program to change the current value of CH0 of the high-speed counter unit to 1000000



■ **Allocation of I/O Numbers**

Signal name	Effective condition	CH0	CH1	CH2	CH3
Current value change request	ON edge	Y105	Y115	Y125	Y135

(Note 1): The above I/O numbers are those for the slot number 1 and the starting word number 10. The I/O numbers actually used vary according to the slot number where the unit is installed and the starting word number.

◆ **KEY POINTS**

- **The current value of the count value can be changed by writing an arbitrary value in the configuration area and turning on the current value change request signal. Values cannot be written in the monitor area directly.**

5.5 Input Time Constant Setting Function

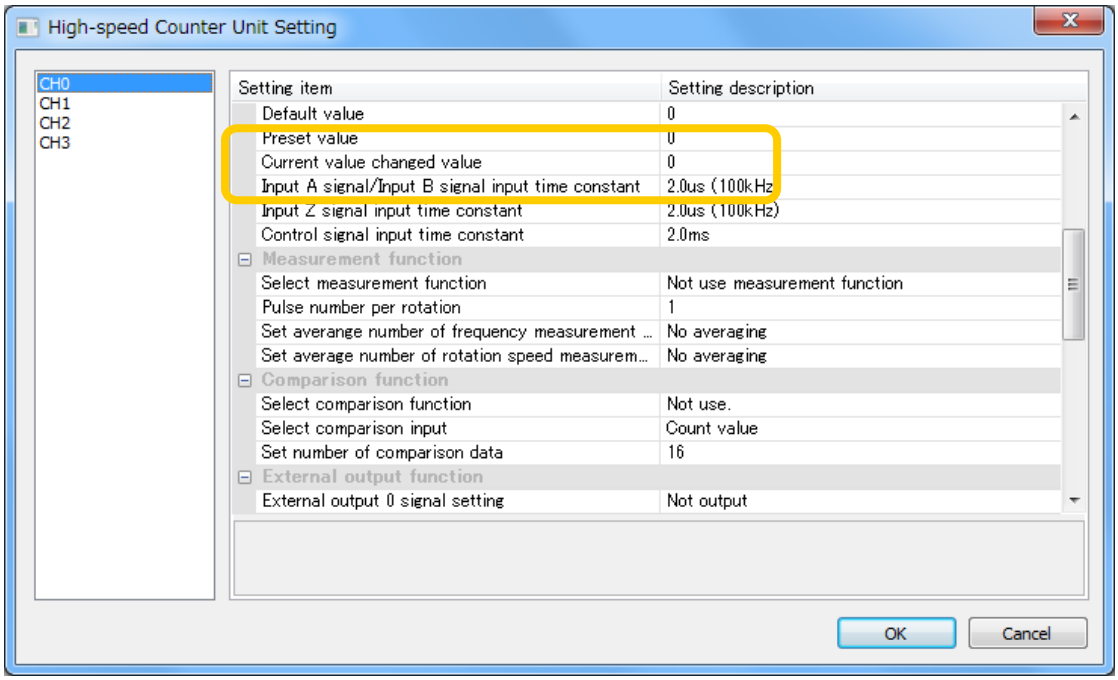
5.5.1 Input Time Constant

- Time constants can be set as noise filters for input signals (phases A, B and Z) and control signals.
- When selecting "No input time constant", input signals are processed without the time constant filter.

■ Count function (Settable for each channel)

Setting item	Settings	Default
Input A signal/Input B signal input time constant	No input time constant / 0.1 us (2 MHz) / 0.2 us (1 MHz) / 0.5 us (500 kHz) / 1.0 us (250 kHz) / 2.0 us (100 kHz) / 10.0 us (10 kHz)	2.0 us (100 kHz)
Input Z signal input time constant		
Control signal input time constant	No input time constant /2 us / 5 us / 10 us / 20 us / 50 us / 100 us / 500 us / 1.0 ms / 2.0 ms / 5.0 ms / 10.0 ms	2.0 ms

■ Example of settings by FPWIN GR7



6
Measurement Function

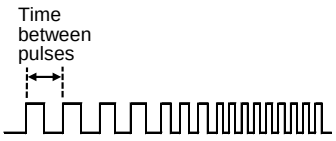
6.1 Overview of Measurement Function

6.1.1 Types of Measurement Function

■ **Measurement function**

- The measurement function is to measure the changes in the count values of the high-speed counter and to output them as frequencies or number of rotations.
- Measuring results are stored in unit memories (UM). They can be read by user programs if necessary.

■ **Types of measurement function**

Type	Operation image	Feature
Frequency measurement function		Measures the time in which the count value changes, and calculates the frequency. Frequency (Hz) = 1/Time between pulses (s) When there is no change in the count value for one second, the result is 0 Hz.
Rotation speed measurement A function		Calculates a rotation speed (rpm) from the time interval of the change in the counter and the specified pulse number per rotation, and stores the measuring result after averaging in the unit memory (UM). Any number can be set for the number of averaging. Measures the time interval of the change in the counter, and calculates the rotation speed (rpm). Rotation speed (rpm) = 60/(Time between pulses x Number of pulses per rotation) The rotation speed measurement A function can be used for the case such as the interval of the change in the counter is large (low-speed pulse). When there is no change in the count value for one second or more, the result is 0 rpm.
Rotation speed measurement B function		Automatically calculates a rotation speed (rpm) from the time interval of the change in the counter and the specified pulse number per rotation, and stores the measuring result after averaging in the unit memory. Any number can be set for the number of averaging. Measures the time which counts the specified pulse number per rotation, and calculates the rotation speed per rotation (rpm). Rotation speed (rpm) = 60/(Time taken for one rotation) The rotation speed measurement B function can be used for the case such as the time interval of the change in the counter is not even. However, when it takes for one second or more for one rotation, the result is 0 rpm.

◆ **KEY POINTS**

- **When the measurement function has been selected in the configuration area, the measuring operation starts once the operation ready done flag turns on.**

6.1.2 Configuration

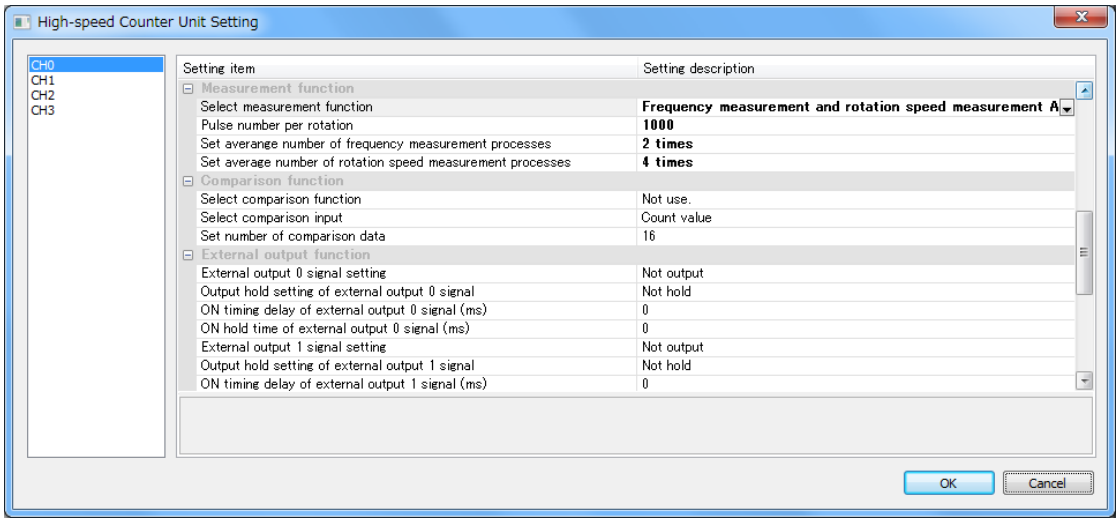
For using the measurement function, set the following items using the configuration menu of tool software FPWIN GR7 or user programs.

■ **Setting area**

Unit memory No. (Hex)	Name	Default	Setting range and description	Unit
UM 00070 UM 00140 UM 00210 UM 002E0	Select measurement function	H0	H0: Not use measurement function H1: Frequency measurement H2: Frequency measurement and rotation speed measurement A H3: Frequency measurement and rotation speed measurement B	—
UM 00071 UM 00072 UM 00141 UM 00142 UM 00211 UM 00212 UM 002E1 UM 002E2	Pulse number per rotation	U1	Set the pulse number for one rotation of the encoder. Setting range: 1 to 1,048,575 (The values out of the setting range are invalid.)	Pulse
UM 00073 UM 00143 UM 00213 UM 002E3	Set averange number of frequency measurement processes	H0	Set the number of averaging of frequency measurement values. H0: No averaging, H1: 2 times, H2: 4 times, H3: 8 times, H4: 16 times, H5: 32 times, H6: 64 times, H7: 128 times	Times
UM 00074 UM 00144 UM 00214 UM 002E4	Set average number of rotation speed measurement processes	H0	Set the number of averaging of rotation speed measurement values. H0: No averaging, H1: 2 times, H2: 4 times, H3: 8 times, H4: 16 times, H5: 32 times, H6: 64 times, H7: 128 times	Times

(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

■ **Example of settings by FPWIN GR7**



6.1.3 Reading Measuring Results

Measuring results are stored in the following area.

■ **Read area**

Unit memory No. (Hex)	Name	Default	Setting range and description	Unit
UM 003A8 UM 003A9	Frequency measurement value (After averaging)	U0	Frequency measurement value after averaging procedure Range: 0 to 20,000,000 Signed 32-bit	Hz
UM 003B8 UM 003B9				
UM 003C8 UM 003C9				
UM 003D8 UM 003D9				
UM 003AA UM 003AB	Rotation speed measurement value (After averaging)	U0	Rotation speed measurement value after averaging procedure Range: -1,200,000,000 to +1,200,000,000 Signed 32-bit	rpm
UM 003BA UM 003BB				
UM 003CA UM 003CB				
UM 003DA UM 003DB				

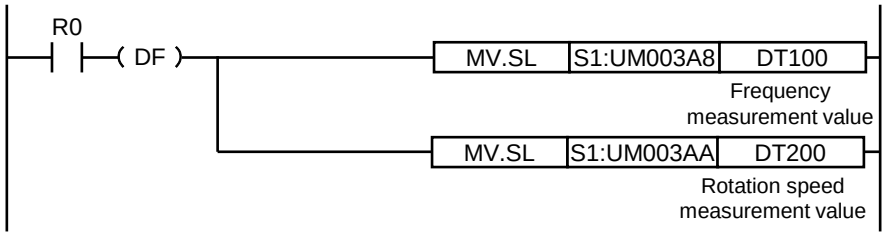
(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

6.1.4 Sample Program

- It can be read at any time.
- The values stored in unit memories can be monitored by the device monitor function of programming tool FPWIN GR7.

■ **Read program**

Example) Program to read the frequency measurement value and the rotation speed measurement value for CH0 of the high-speed counter unit installed in the slot number 1



7

Comparison Function

7.1 Overview of Comparison Function

7.1.1 Types of Comparison Function

■ Comparison function

- Compares the current value of the high-speed counter with a specified target value, and reflects the matched value in the comparison match flag.
- There are two methods, which are the target value match comparison and the band comparison.
- Comparison results can be output to external devices from the unit.

■ Comparison match function specifications

Item	Description	Remark
No. of comparison data	Max. 16 data per channel (Comparison data 0 ~ Comparison data 15)	
Comparison match flag	Max. 16 points per channel (Comparison match 0 flag to Comparison match F flag) Read as input relays (X) by user programs. Multiple comparison match flags can be set for single comparison data.	
Comparison method	Target value match comparison Sets or resets the comparison match flag when the elapsed value matches the target value.	
	Band comparison Turns on or off the comparison match flag when the elapsed value is in the range of specified lower and upper limits.	
External output	Max. 2 points per channel The comparison match 0 flag can be allocated to the external output 0 terminal of the unit. The comparison match 1 flag can be allocated to the external output 1 terminal of the unit.	
	The following settings are available only when the band comparison function is used. ON delay timing: 0 to 1,000 ms ON hold time: 0 to 1,000 ms	
	Forced output function The outputs of external output 0 terminal and external output 1 terminal can be controlled on the ladder monitor or device monitor of tool software.	

■ I/O Allocation

Signal name	CH0	CH1	CH2	CH3
Comparison match flag	X110-X11F	X130-X13F	X150-X15F	X170-X17F

(Note 1): The above I/O numbers are those for the slot number 1 and the starting word number 10. The I/O numbers actually used vary according to the slot number where the unit is installed and the starting word number.

◆ **KEY POINTS**

- **Only the comparison match 0 flag or comparison match 1 flag can be set as the external output of the high-speed counter unit.**
- **The default for the external output 0 and 1 settings is "Not output". Change the settings in the configuration menu as necessary.**
- **There is no need to arrange comparison data in ascending or descending order.**

7.1.2 Target Value Match Comparison and Band Comparison

- The main difference is as below.
- The comparison methods can be selected for each channel.

■ **Main difference in characteristics**

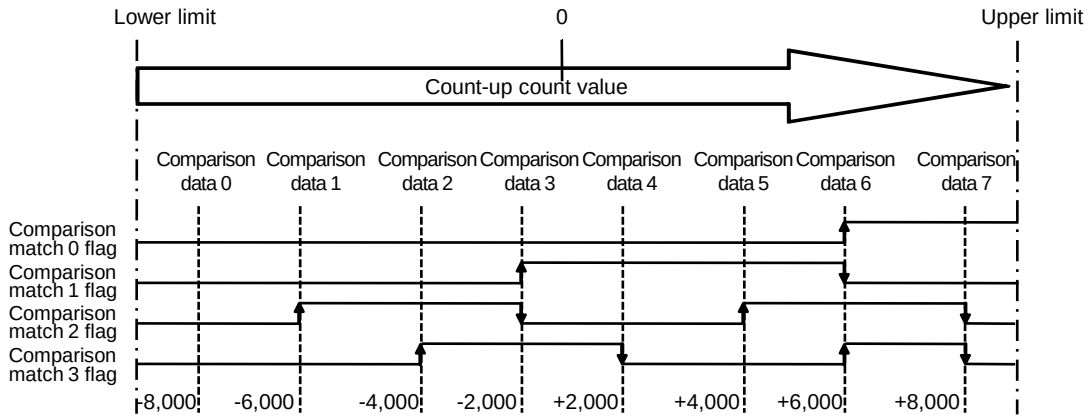
Item	Target value match comparison	Band comparison
Setting of comparison value data	Comparison value data is specified as points.	Comparison value data is specified with upper and lower limits.
Setting when comparison value data matches	The operation when reaching the target value is selected from the following four patterns. Sets when the values are matched at the time of addition. Resets when the values are matched at the time of addition. Sets when the values are matched at the time of subtraction. Resets when the values are matched at the time of subtraction.	Specify ON or OFF for the state of the comparison match flag when the current value is in a specified band.
Operation when comparison value data matches	The operations when the value reaches the same comparison data may differ between the cases of addition and subtraction.	The same operation is performed for the same comparison data in the cases of both addition and subtraction.
Time setting of external output signal	The settings listed on the right are not available.	ON delay timing: 0 to 1,000 ms ON hold time: 0 to 1,000 ms The ON delay timing and ON hold time can be specified in combination.

7.2 Operation of Target Value Match Function

7.2.1 Examples of Linear counter Settings

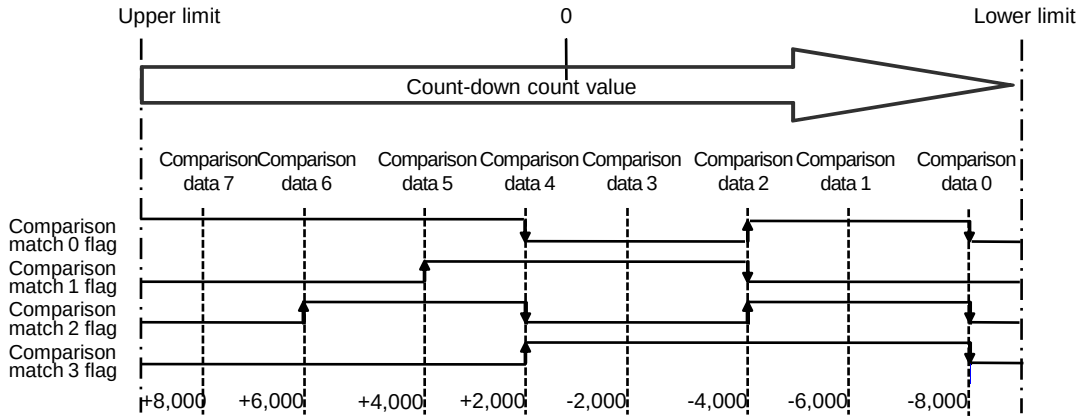
■ **Example of comparison match flag operation when counting up.**

Operates according to the settings of addition set pattern and addition reset pattern when the current value matches the comparison data.



■ **Example of comparison match flag operation when counting down.**

Operates according to the settings of subtraction set pattern and addition reset pattern when the current value matches the comparison data.



■ **Examples of output pattern settings**

Comparison data	Target value	Output pattern	Comparison match 0 flag	Comparison match 1 flag	Comparison match 2 flag	Comparison match 3 flag
0	-8,000	Addition set pattern				
		Addition reset pattern				
		Subtraction set pattern				
		Subtraction reset pattern	○		○	○
1	-6,000	Addition set pattern			○	
		Addition reset pattern				
		Subtraction set pattern				
		Subtraction reset pattern				
2	-4,000	Addition set pattern				○
		Addition reset pattern				
		Subtraction set pattern	○		○	
		Subtraction reset pattern		○		
3	-2,000	Addition set pattern		○		
		Addition reset pattern			○	
		Subtraction set pattern				
		Subtraction reset pattern				
4	+2,000	Addition set pattern				
		Addition reset pattern				○
		Subtraction set pattern				○
		Subtraction reset pattern	○		○	
5	+4,000	Addition set pattern			○	
		Addition reset pattern				
		Subtraction set pattern		○		
		Subtraction reset pattern				
6	+6,000	Addition set pattern	○			○
		Addition reset pattern		○		
		Subtraction set pattern			○	
		Subtraction reset pattern				
7	+8,000	Addition set pattern				
		Addition reset pattern			○	○
		Subtraction set pattern				
		Subtraction reset pattern				

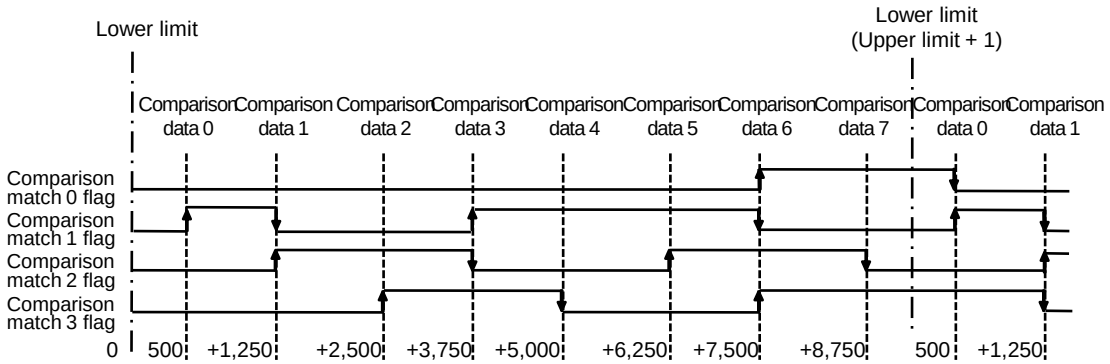
◆ **KEY POINTS**

- **The operation of comparison match flag when the count value reaches the target value can be changed depending on the cases of addition and subtraction.**
- **If the contents of comparison data 0 to 15 are overlapped and the specified reset conditions are different, the priority of data is in the following order. (High) 0 > 1 > 2 > 3 > 4 > 5 > 6 > 7 > 8 > 9 > 10 > 11 > 12 > 13 > 14 > 15 (Low)**

7.2.2 Examples of Ring Counter Settings

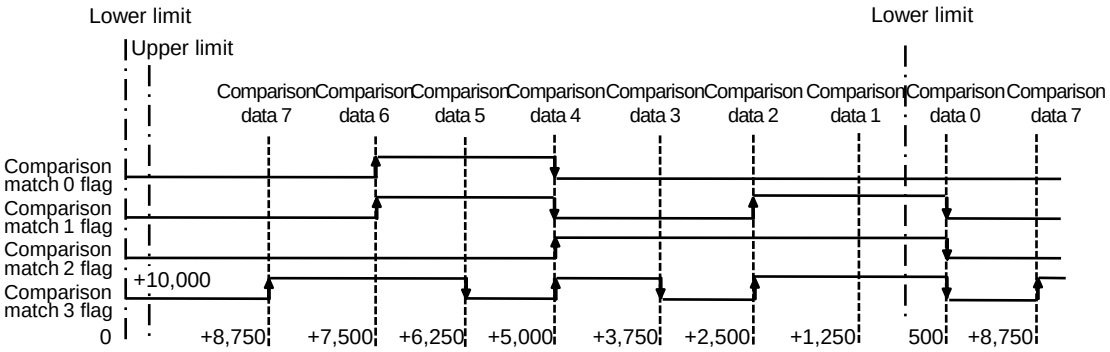
■ **Comparison match flag operation when counting up**

Operates according to the settings of addition set pattern and addition reset pattern when the current value matches the comparison data.



■ **Comparison match flag operation when counting down**

Operates according to the settings of subtraction set pattern and addition reset pattern when the current value matches the comparison data.



◆ **KEY POINTS**

- **For the ring counter, comparison data is set for the area including the upper and lower limits in which the count value is rolled over, and set patterns can be set.**

■ **Examples of output pattern settings**

Comparison data	Target value	Output pattern	Comparison match 0 flag	Comparison match 1 flag	Comparison match 2 flag	Comparison match 3 flag
0	+500	Addition set pattern		○		
		Addition reset pattern	○			
		Subtraction set pattern				
		Subtraction reset pattern		○	○	○
1	+1,250	Addition set pattern			○	
		Addition reset pattern		○		○
		Subtraction set pattern				
		Subtraction reset pattern				
2	+2,500	Addition set pattern				○
		Addition reset pattern				
		Subtraction set pattern		○		○
		Subtraction reset pattern				
3	+3,750	Addition set pattern		○		
		Addition reset pattern			○	
		Subtraction set pattern				
		Subtraction reset pattern				○
4	+5,000	Addition set pattern				
		Addition reset pattern				○
		Subtraction set pattern			○	○
		Subtraction reset pattern	○	○		
5	+6,250	Addition set pattern			○	
		Addition reset pattern				
		Subtraction set pattern				
		Subtraction reset pattern				○
6	+7,500	Addition set pattern	○			○
		Addition reset pattern		○		
		Subtraction set pattern	○	○		
		Subtraction reset pattern				
7	+8,750	Addition set pattern				
		Addition reset pattern			○	
		Subtraction set pattern				○
		Subtraction reset pattern				

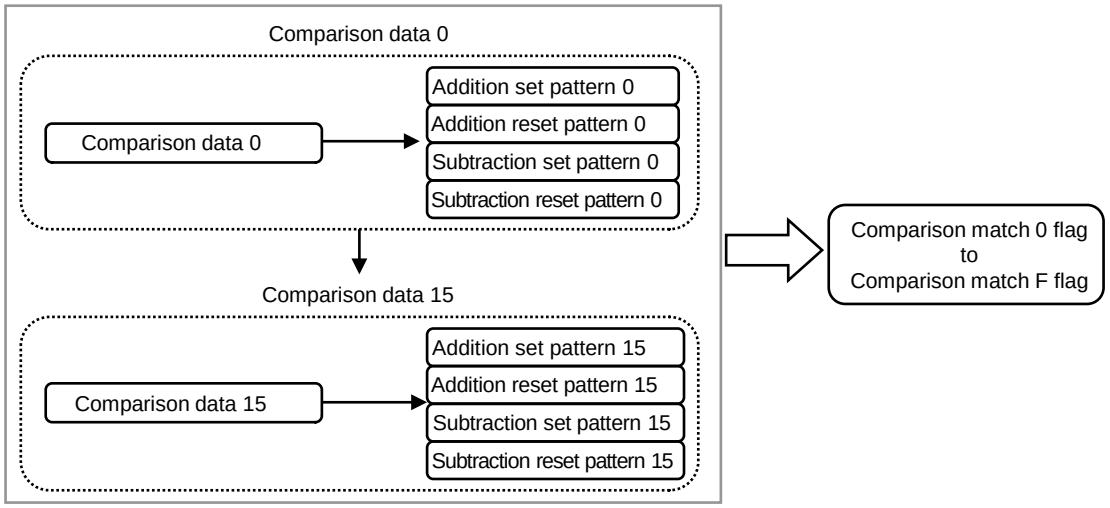
◆ **KEY POINTS**

- **The operation of comparison match flag when the count value reaches the target value can be changed depending on the cases of addition and subtraction.**
- **If the contents of comparison data 0 to 15 are overlapped and the specified reset conditions are different, the priority of data is in the following order. (High) 0 > 1 > 2 > 3 > 4 > 5 > 6 > 7 > 8 > 9 > 10 > 11 > 12 > 13 > 14 > 15 (Low)**

7.2.3 Configuration of Target Value Match Comparison

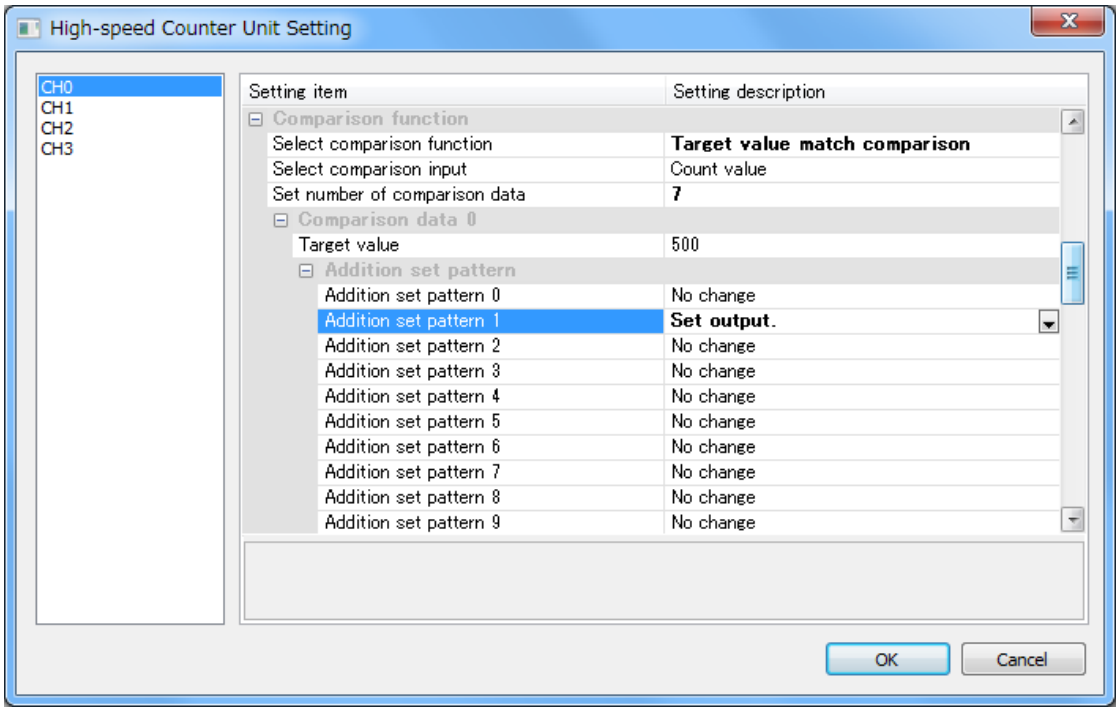
■ **Overview of setting items**

- For each comparison data, specify whether to set or reset each flag when the current value matches the target value.
- Multiple comparison match flags can be set for one comparison data.
- Different flag operations can be set depending on the count direction when the values are matched (at the time of addition or subtraction).



Setting for Target value match comparison

■ **Example of settings by FPWIN GR7**


High-speed Counter Unit Setting
CH0
CH1
CH2
CH3
Setting item
Setting description
Comparison function
Select comparison function
Target value match comparison
Select comparison input
Count value
Set number of comparison data
7
Comparison data 0
Target value
500
Addition set pattern
Addition set pattern 0
No change
Addition set pattern 1
Set output.
Addition set pattern 2
No change
Addition set pattern 3
No change
Addition set pattern 4
No change
Addition set pattern 5
No change
Addition set pattern 6
No change
Addition set pattern 7
No change
Addition set pattern 8
No change
Addition set pattern 9
No change
OK
Cancel

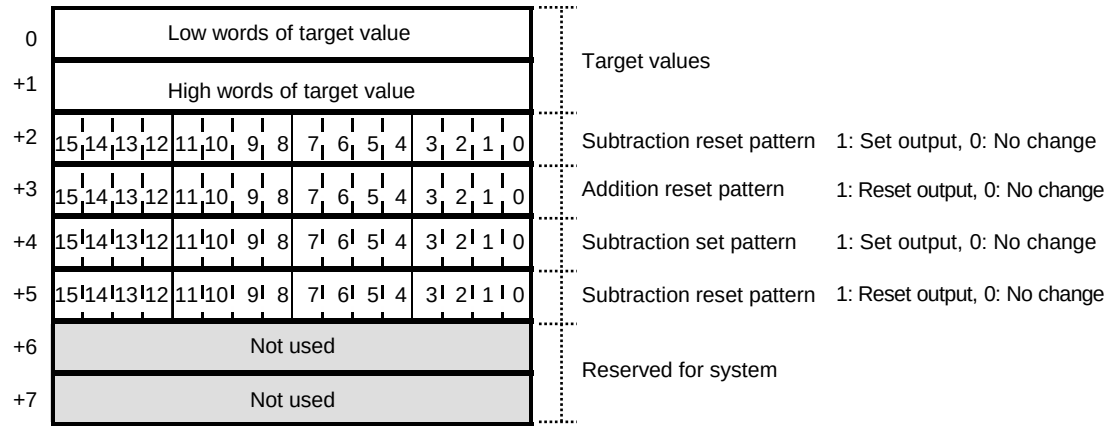
■ **Pattern of storage in unit memories (UM)**

- Set data is stored in 8-word blocks of corresponding unit memories in the following format.
- When using user programs, set data in corresponding unit memory numbers.

Example 1) For the comparison data 0 of CH0, it is allocated to UM00080 to UM00087.

Example 2) For the comparison data 1 of CH0, it is allocated to UM00088 to UM0008F.

- The bit numbers 0 to 15 in the areas of +2 to +5 in the figure below correspond to the comparison match 0 flag to F flag.



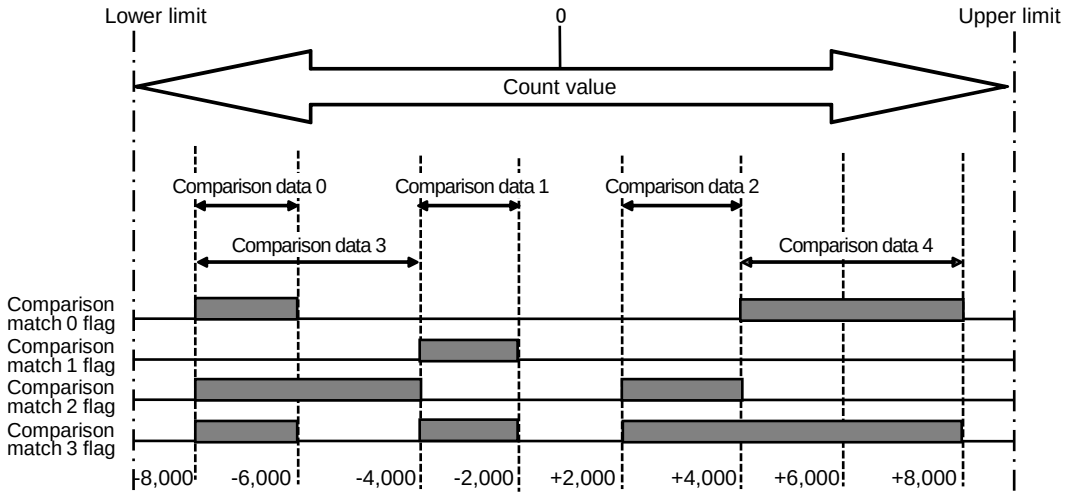
◆ **REFERENCE**

- **For details of unit memory numbers, refer to 11.4 Unit Memory Detailed Specifications.**

7.3 Operation of Band Comparison Function

7.3.1 Examples of Linear counter Settings

■ **Operation of band comparison match flag**



■ **Examples of output pattern settings**

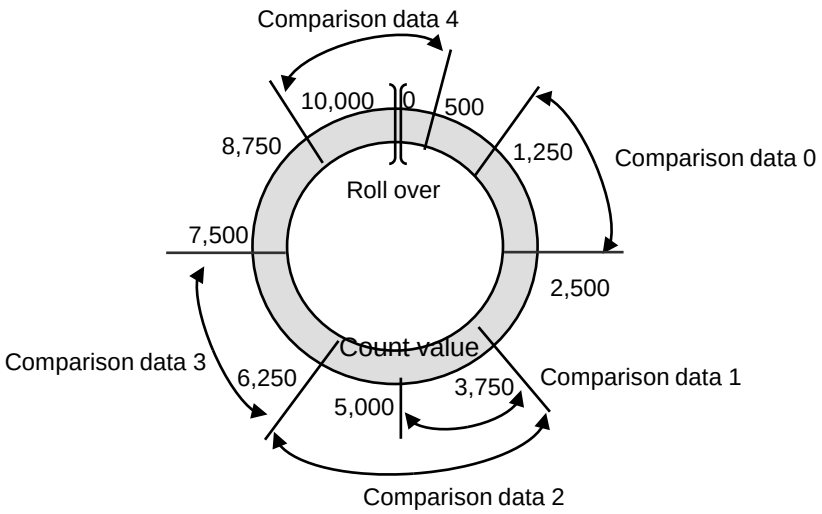
Comparison data	Band comparison value		Output pattern	Comparison match 0 flag	Comparison match 1 flag	Comparison match 2 flag	Comparison match 3 flag
	Lower limit	Upper limit					
0	-8,000	-6,000	Set pattern	ON	OFF	ON	ON
1	-4,000	-2,000	Set pattern	OFF	ON	OFF	ON
2	+2,000	+4,000	Set pattern	OFF	OFF	ON	ON
3	-8,000	-4,000	Set pattern	OFF	OFF	ON	OFF
4	+4,000	+8,000	Set pattern	ON	OFF	OFF	ON

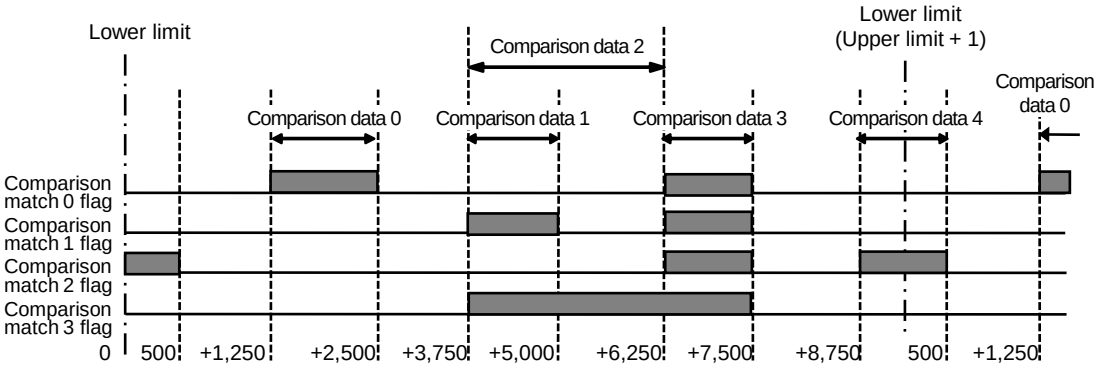
◆ **KEY POINTS**

- **The output is off in the areas of the bands in which comparison data is not set.**
- **Multiple comparison data can be set for the same band.**
- **If the contents of comparison data 0 to 15 are overlapped and the specified reset conditions are different, the priority of data is in the following order. (High) 0 > 1 > 2 > 3 > 4 > 5 > 6 > 7 > 8 > 9 > 10 > 11 > 12 > 13 > 14 > 15 (Low)**

7.3.2 Examples of Ring Counter Settings

■ **Operation of band comparison match flag**





■ **Examples of output pattern settings**

Comparison data	Band comparison value		Output pattern	Comparison match 0 flag	Comparison match 1 flag	Comparison match 2 flag	Comparison match 3 flag
	Lower limit	Upper limit					
0	+1,250	2,500	Set pattern	ON	OFF	OFF	OFF
1	+3,750	+5,000	Set pattern	OFF	ON	OFF	ON
2	+3,750	+7,500	Set pattern	OFF	OFF	OFF	ON
3	+6,250	+7,500	Set pattern	ON	ON	ON	ON
4	+8,750	+500	Set pattern	OFF	OFF	ON	OFF

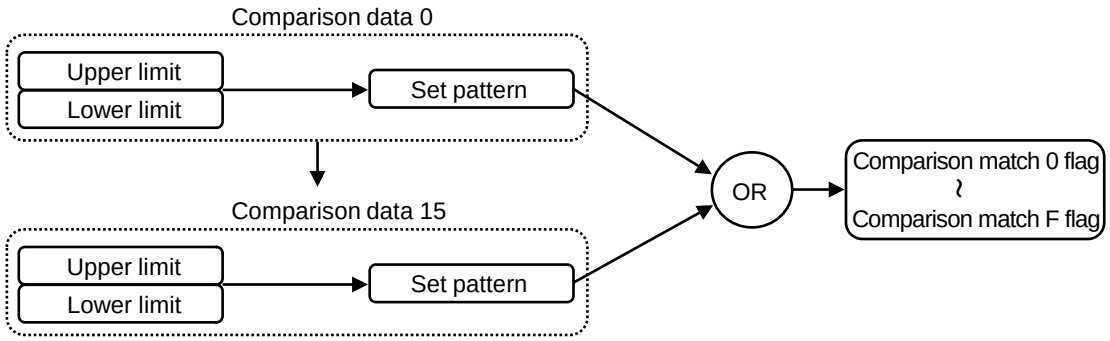
◆ KEY POINTS

- **For the ring counter, comparison data is set for the area including the upper and lower limits in which the count value is rolled over, and set patterns can be set.**

7.3.3 Configuration of Band Comparison

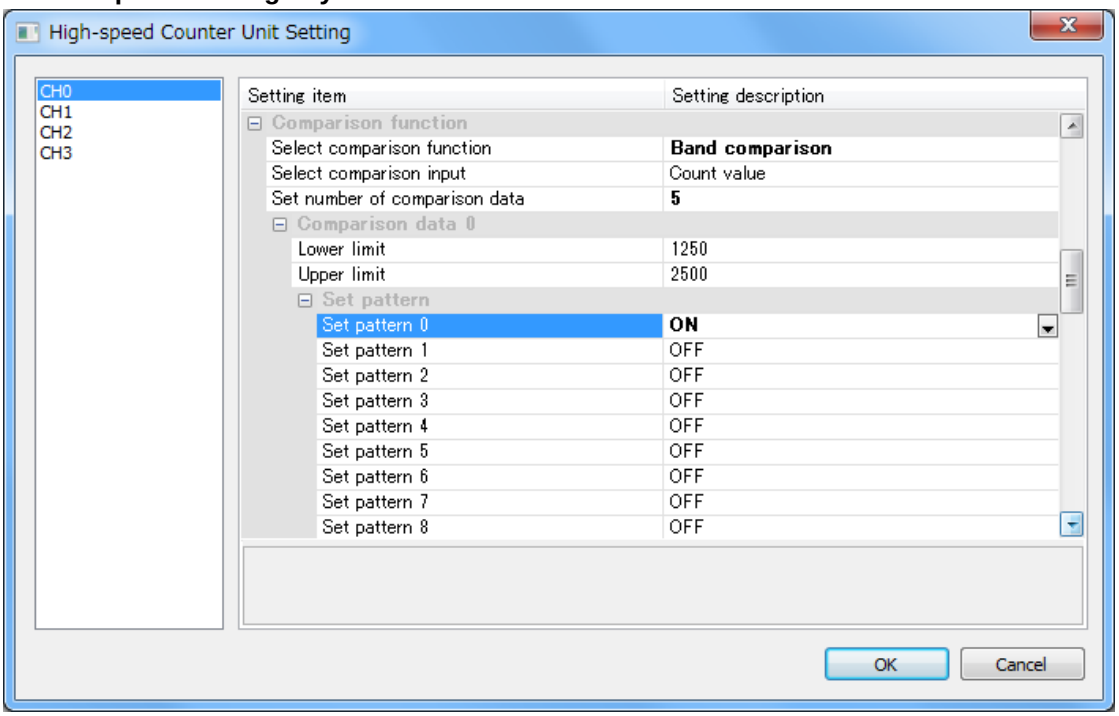
■ Overview of setting items

- When the current value exists between the lower and upper limits of each comparison data, the ON or OFF state of each flag is set for each comparison data.
- Multiple comparison match flags can be set for one comparison data.
- Multiple comparison data can be set for the same band.



Setting for Band comparison

■ Example of settings by FPWIN GR7



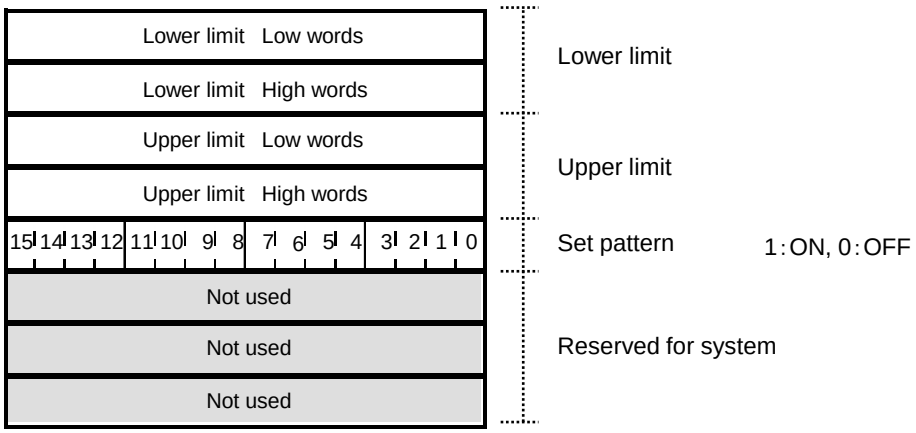
■ **Pattern of storage in unit memories (UM)**

- Set data is stored in 8-word blocks of corresponding unit memories in the following format.
- When using user programs, set data in corresponding unit memory numbers.

Example 1) For the comparison data 0 of CH0, it is allocated to UM00080 to UM00087.

Example 2) For the comparison data 1 of CH0, it is allocated to UM00088 to UM0008F.

- The bit numbers 0 to 15 in the area of +4 in the figure below correspond to the comparison match 0 flag to F flag.



◆ **REFERENCE**

- **For details of unit memory numbers, refer to 11.4 Unit Memory Detailed Specifications.**

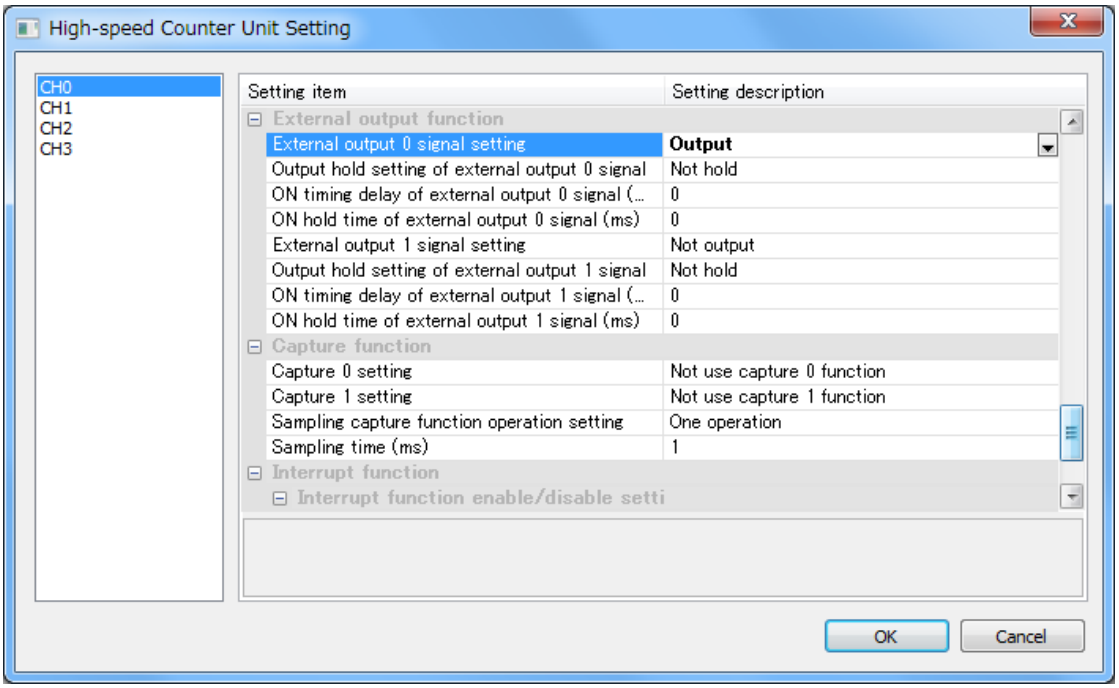
7.4 External Output

7.4.1 Overview of External Output Function

■ External output function

- The result of comparison is reflected in 16 flags (comparison match 0 flag to comparison match F flag), and the two of them (comparison match 0 flag and comparison match 1 flag) can be retrieved as external outputs by being allocated to the external output terminals of the unit.
- The configuration menu of FPWIN GR7 or the corresponding unit memories (UM) are used for the allocation.

■ Example of settings by FPWIN GR7



■ **Setting items and corresponding unit memory numbers**

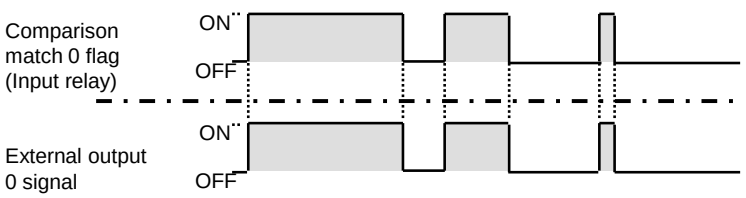
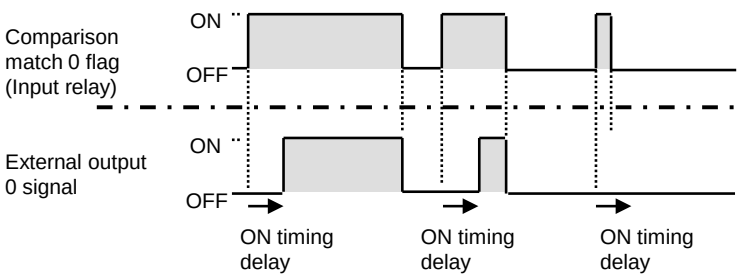
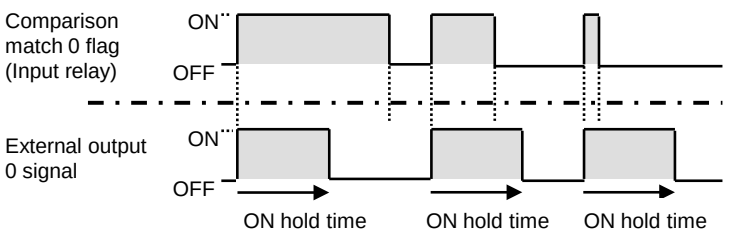
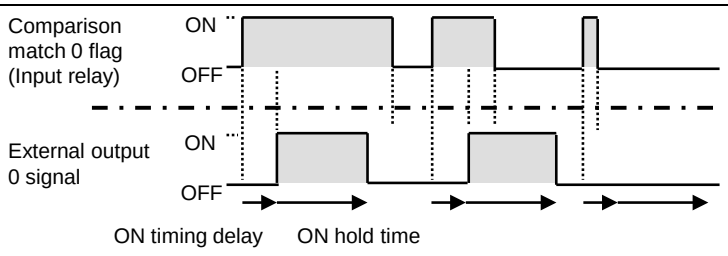
Unit memory No. (Hex)	Name	Default	Setting range and description	Unit
UM 00100 UM 001D0 UM 002A0 UM 00370	External output 0 signal setting	H0	Set whether or not to output the comparison match 0 flag to the external output 0 signal. H0: Not output H1: Output	—
UM 00101 UM 001D1 UM 002A1 UM 00371	Output hold setting of external output 0 signal	H0	Set whether or not to hold the output signal in the program mode when an error occurs. H0: Not hold H1: Hold	—
UM 00102 UM 001D2 UM 002A2 UM 00372	External output 0 signal ON timing delay (Available when band comparison function is used)	0	Set the ON timing delay of external output 0 signal. Setting range: 0 to 1,000(The values out of the setting range are invalid.)	ms
UM 00103 UM 001D3 UM 002A3 UM 00373	External output 0 signal ON hold time (Available when band comparison function is used)	0	Set the ON hold time of external output 0 signal. Setting range: 0 to 1,000 (The values out of the setting range are invalid.)	ms
UM 00104 UM 001D4 UM 002A4 UM 00374	External output 1 signal setting	H0	Set whether or not to output the comparison match 1 flag to the external output 1 signal. H0: Not output H1: Output	—
UM 00105 UM 001D5 UM 002A5 UM 00375	Output hold setting of external output 1 signal	H0	Set whether or not to hold the output signal in the program mode when an error occurs. H0: Not hold H1: Hold	—
UM 00106 UM 001D6 UM 002A6 UM 00376	External output 1 signal ON timing delay (Available when band comparison function is used)	0	Set the ON timing delay of external output 1 signal. Setting range: 0 to 1,000 (The values out of the setting range are invalid.)	ms
UM 00107 UM 001D7 UM 002A7 UM 00377	External output 1 signal ON hold time (Available when band comparison function is used)	0	Set the ON hold time of external output 1 signal. Setting range: 0 to 1,000 (The values out of the setting range are invalid.)	ms

(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

7.4.2 Output Pattern Setting (Only for Band Comparison)

When using the band comparison function, the ON timing delay time or ON hold time can be set for output signals.

■ **Operational difference between settings**

ON hold time	ON timing delay	Timing chart of comparison match flag and external output
0	0	
0	1 to 1,000 ms	
1 to 1,000 ms	0	
1 to 1,000 ms	1 to 1,000 ms	

7.4.3 Forced Output Function

- The outputs of external output 0 terminal and external output 1 terminal can be controlled on the ladder monitor or device monitor of tool software FPWIN GR7. They can be also turned on or off by user programs.
- It can be used for the confirmation of wirings.

■ **I/O Allocation of external output terminals**

Signal name	Effective condition	CH0	CH1	CH2	CH3
External output 0 forced ON	Level	Y109	Y119	Y129	Y139
External output 0 forced OFF	Level	Y10A	Y11A	Y12A	Y13A
External output 1 forced ON	Level	Y10B	Y11B	Y12B	Y13B
External output 1 forced OFF	Level	Y10C	Y11C	Y12C	Y13C

(Note 1): The above I/O numbers are those for the slot number 1 and the starting word number 10. The I/O numbers actually used vary according to the slot number where the unit is installed and the starting word number.

◆ **KEY POINTS**

- **The above forced output function is a function of the high-speed counter unit. The forced I/O function of programming tool FPWIN GR7 is not used.**

8

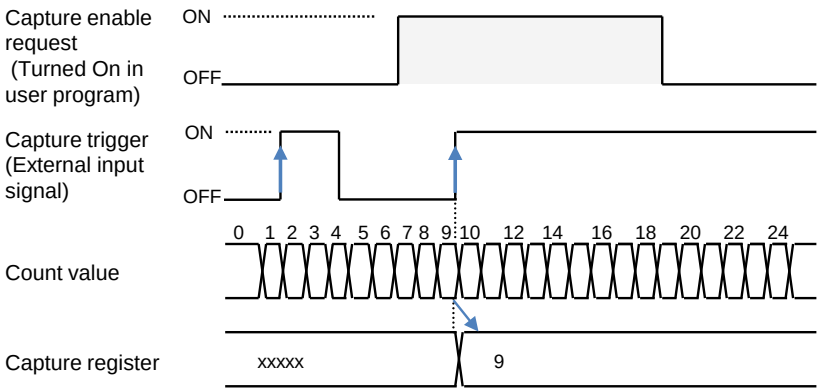
Capture Function

8.1 Overview of Functions

8.1.1 Types of Capture Function

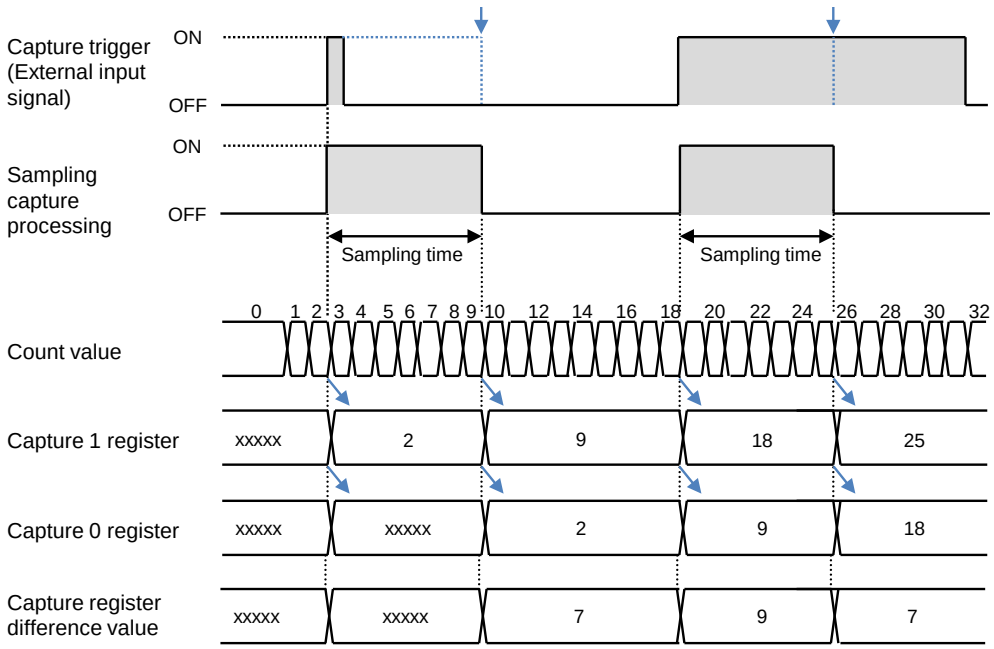
■ Capture function

- Stores the count value at the time an external input signal changes into the unit memory (capture register) of the high-speed counter unit.



■ Sampling capture function

- Stores the count values during a specified sampling time form the time an external input signal changes into the unit memory (capture register) of the high-speed counter unit.
- The count values for the sampling time can be monitored by reading the difference value register.



8.1.2 Restrictions on Combinations

Available conditions vary by functions.

■ **Comparison of functions**

<table>
<tr><th colspan="2">Item</th><th>Capture function</th><th>Sampling capture function</th></tr>
<tr><td colspan="2" rowspan="2">Usable number of points</td><td>Max. 2 points</td><td>Max. 1 point</td></tr>
<tr><td colspan="2">The capture function cannot be used when using the sampling capture function.</td></tr>
<tr><td colspan="2" rowspan="2">Used unit memory (UM) area (Note 1)</td><td>Individually usable;
Capture 0 register: 1 point (2 words)
Capture 1 register: 1 point (2 words)</td><td>Use Capture 0 register: 1 point (2 words)</td></tr>
<tr><td colspan="2">Difference value register (Value of Capture 1 register - Value of Capture 0 register): 1 point (2 words)</td></tr>
<tr><td colspan="2">Buffer function (Note 2)</td><td colspan="2">Data in the capture registers are shifted to the buffer area in sequence when executing the capture function.
For the capture 0 register, capture 1 register, difference value register (when activating the capture 0) and difference value register (when activating the capture 1), each 60-point (120-word) area is secured.</td></tr>
<tr><td colspan="2">Capture function valid condition (Note 2)</td><td>The capture function is valid while the capture enable request signals (Y7, Y17, Y27, Y37) is on using user programs.</td><td>The capture function is always valid.</td></tr>
<tr><td rowspan="4">Capture trigger (Note 1)</td><td colspan="2">Allocated in the configuration menu of tool software.</td><td></td></tr>
<tr><td>Control signal 0</td><td>Used as a trigger for capture 0 or capture 1.</td><td>Used as a tirgger for both capure 0 and capture 1.</td></tr>
<tr><td>Control signal 1</td><td>Used as a trigger for capture 0 or capture 1.</td><td>Not used</td></tr>
<tr><td>Capture trigger signal valid condition</td><td>Activated when any of the following conditions is met.
● Leading edge of control signal
● Trailing edge of control signal
It is possible to allocate one control signal to different capture numbers as the signals of leading edge and trailing edge respectively.</td><td>Activated when any of the following conditions is met.
● Control signal (Positive logic)
● Control signal (Negative logic)
● Capture enable request by user programs (Y7, Y17, Y27, Y37)</td></tr>
<tr><td colspan="2">Capture data memory area clear (Note 3)</td><td colspan="2">Capture 0 register and capture 1 register can be cleared individually using user programs.
Buffer areas can be reset at the same time.</td></tr>
<tr><td colspan="2">Capture done flag clear (Note 3)</td><td colspan="2">It is automatically cleared at the time of I/O refresh.
Capture 0 register and capture 1 register can be cleared individually using user programs.</td></tr>
</table>

(Note 1) Functions and capture trigger signals to be used are set in the configuration menu of tool software or user programs.

(Note 2) The buffer function and capture function valid conditions are available from thei high-speed counter unit Ver.1.2.

(Note 3) The capture value clear request and capture done flag clear request signals are available from the high-speed counter unit Ver.1.2. They can be set in user programs.

8.1.3 Configuration

- For using the capture function or sampling capture function, set the following items using the configuration menu of tool software or user programs.
- Set the signal allocated to the trigger signal for executing capturing and the number of operations. For the sampling capture, also set the sampling time.

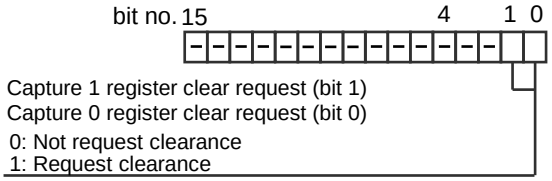
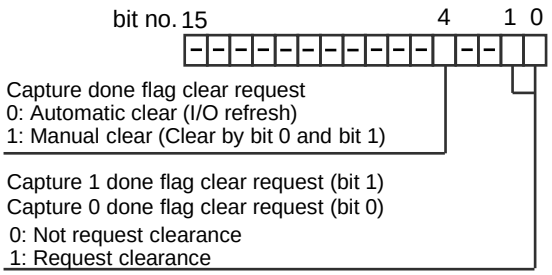
■ **Setting area**

Unit memory No. (Hex)	Name	Default	Setting range and description	Unit
UM 00110 UM 001E0 UM 002B0 UM 00380	Capture 0 setting	H0	Make the setting for the capture function or sampling capture function. H0: Not use capture 0 function H1: Capture function at rising edge of control 0 signal H2: Capture function at trailing edge of control 0 signal H3: Capture function at rising edge of control 1 signal H4: Capture function at trailing edge of control 1 signal H5: Control 0 signal positive logic sampling capture function H6: Control 0 signal negative logic sampling capture function H7: Control 1 signal positive logic sampling capture function H8: Control 1 signal negative logic sampling capture function H9: Output relay (Y relay) sampling capture function	-
UM 00111 UM 001E1 UM 002B1 UM 00381	Capture 1 setting	H0	Make the setting for the capture function or sampling capture function. H0: Not use capture 1 function H1: Capture function at rising edge of control 0 signal H2: Capture function at trailing edge of control 0 signal H3: Capture function at rising edge of control 1 signal H4: Capture function at trailing edge of control 1 signal However, this setting area is invalid when the sampling capture function (H5 to H9) is selected in the capture 0 setting.	-
UM 00112 UM 001E2 UM 002B2 UM 00382	Capture function operation setting	H0	Make the setting for the capture function or sampling capture function. H0: One operation H1: Continuous operation	-
UM 00113 UM 001E3 UM 002B3 UM 00383	Sampling time	1	Set the sampling time for using the sampling capture function. Setting range: 1 to 65,535 (The values out of the setting range are invalid.)	ms

(Note 1) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

☛ next page

■ **Setting area**

Unit memory No. (Hex)	Name	Default	Setting range and description	Unit
UM 00114 UM 001E4 UM 002B4 UM 00384	Capture value clear request	H0	● Clears values stored in the capture registers and capture register buffers. ● To clear the capture 0 register, turn off, on and off the bit 0 of the unit memory. To clear the capture 1 register, turn off, on and off the bit 1 of the unit memory. ● Clears the areas of capture 0 register, capture 0 register buffer and register difference value buffer when requesting the capture 0 by executing the clearance of the capture 0 register. ● Clears the areas of capture 1 register, capture 1 register buffer and register difference value buffer when requesting the capture 1 by executing the clearance of the capture 1 register. 	-
UM 00115 UM 001E5 UM 002B5 UM 00385	Capture done flag clear request (Edge type)	H0	● The capture done flag is automatically reset at the time of I/O refresh at the default setting. ● It is used to reset the capture 0 done flag and capture 1 done flag using user programs. ● To reset the capture 0 done flag, write H11 and then H10. To reset the capture 1 done flag, write H12 and then H10. 	-

(Note 1) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

(Note 2) The capture value clear request and capture done flag clear request signals are available from the high-speed counter unit Ver.1.2. They can be set in user programs.

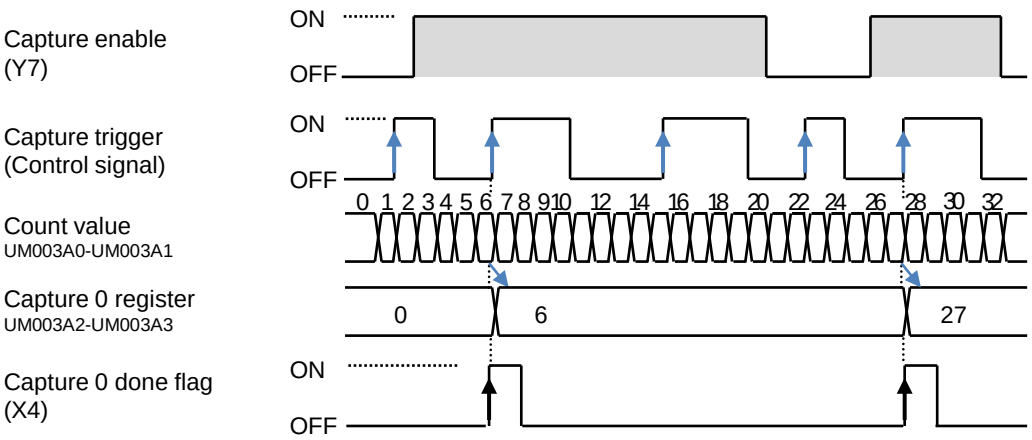
(Note 3) Even if the capture value clear request is executed, the number of completed capture operations in the buffer area will not be cleared. The number of completed capture operations will be cleared when the capture enable request (Y7) or the sampling capture function is activated.

8.2 Operations of Capture Function

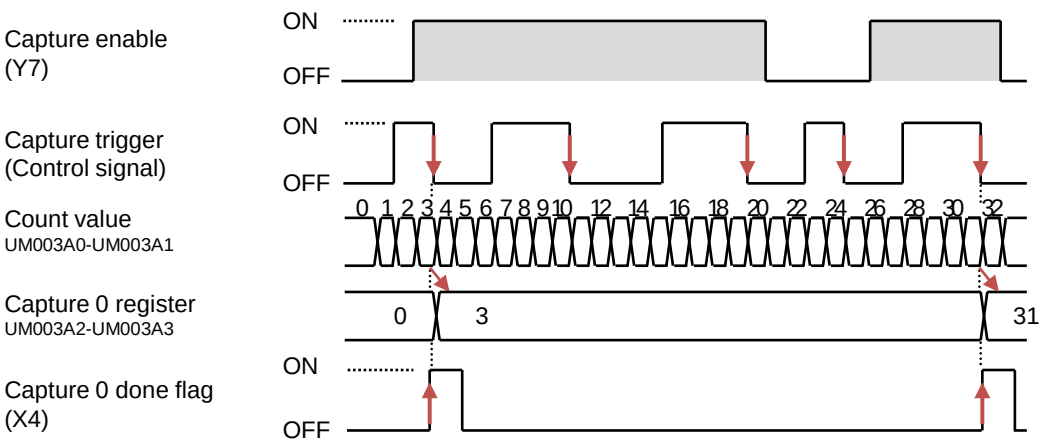
8.2.1 One operation

- Capturing is executed when the first capture trigger condition (control signal) is met while the capture function is enabled by the capture enable request signal (Y7).
- The operation changes as follows according to the settings (leading and trailing edges) of the valid control signal.

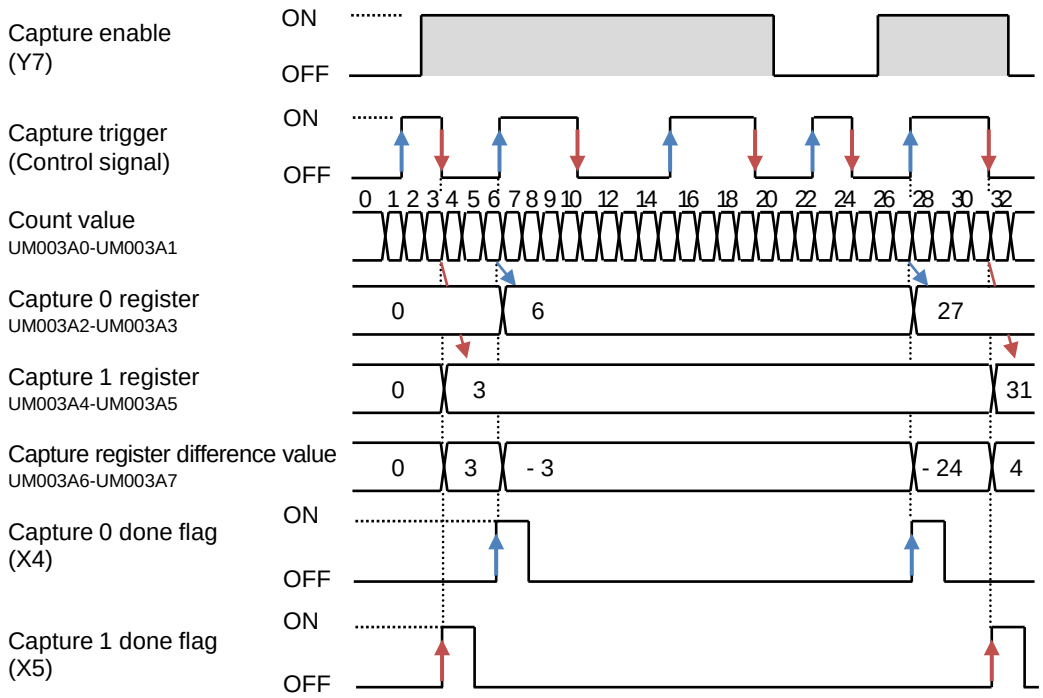
■ **When "Leading edge" is set as the capture trigger condition**



■ **When "Trailing edge" is set as the capture trigger condition**



■ **When "Leading edge" and "Trailing edge" of the same signal are set as the capture trigger condition**



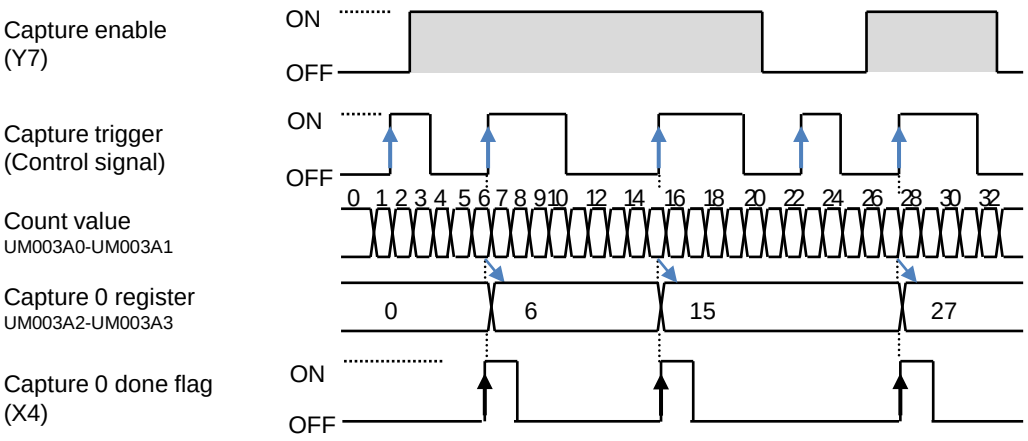
◆ **KEY POINTS**

- **The values ((Capture 1 register) - (Capture 0 register)) are always stored as capture register difference values. The signs for the values of capture difference value register change according to the sequence of the capture enable signal (output Y contact) and the capture trigger (control signal).**

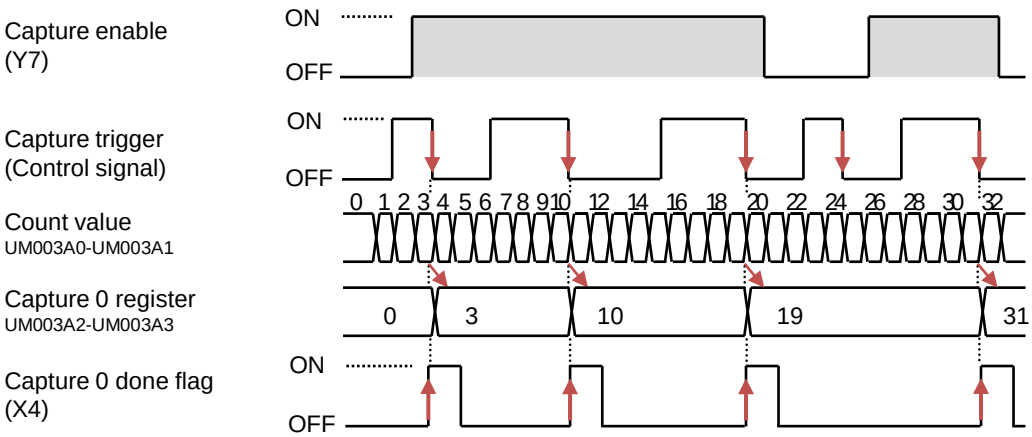
8.2.2 Continuous Operation

- Capturing is executed every time the capture trigger condition (control signal) is met while the capture function is enabled by the capture enable request signal (Y7).
- The operation changes as follows according to the settings (leading and trailing edges) of the valid control signal.

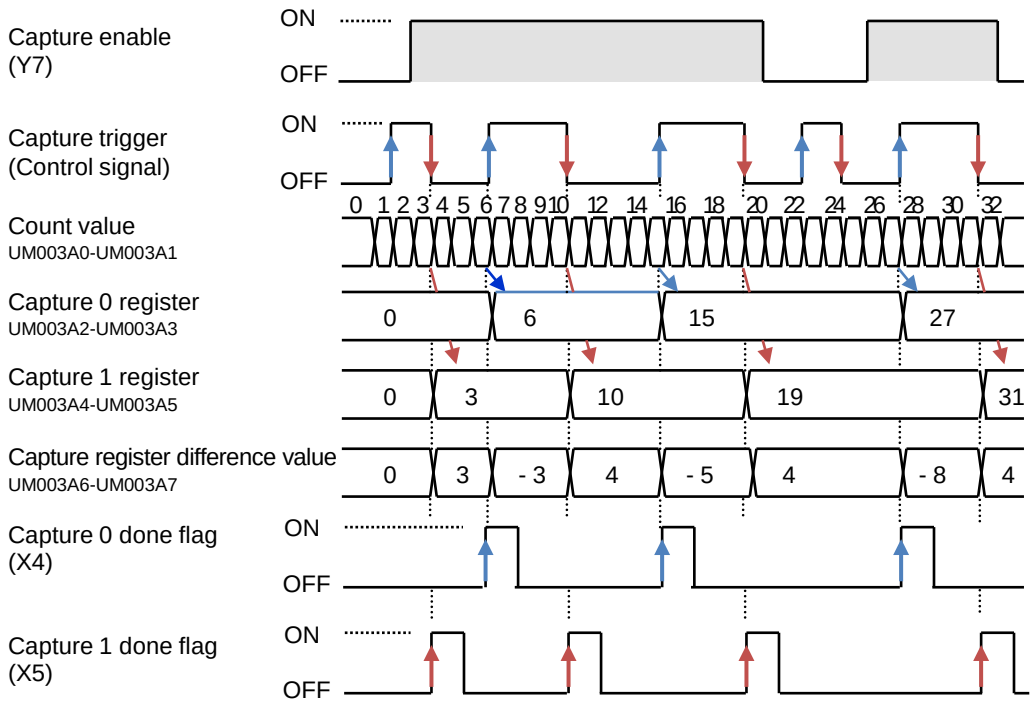
■ **When "Leading edge" is set as the capture trigger condition**



■ **When "Trailing edge" is set as the capture trigger condition**



■ **When "Leading edge" and "Trailing edge" of the same signal are set as the capture trigger condition**



◆ **KEY POINTS**

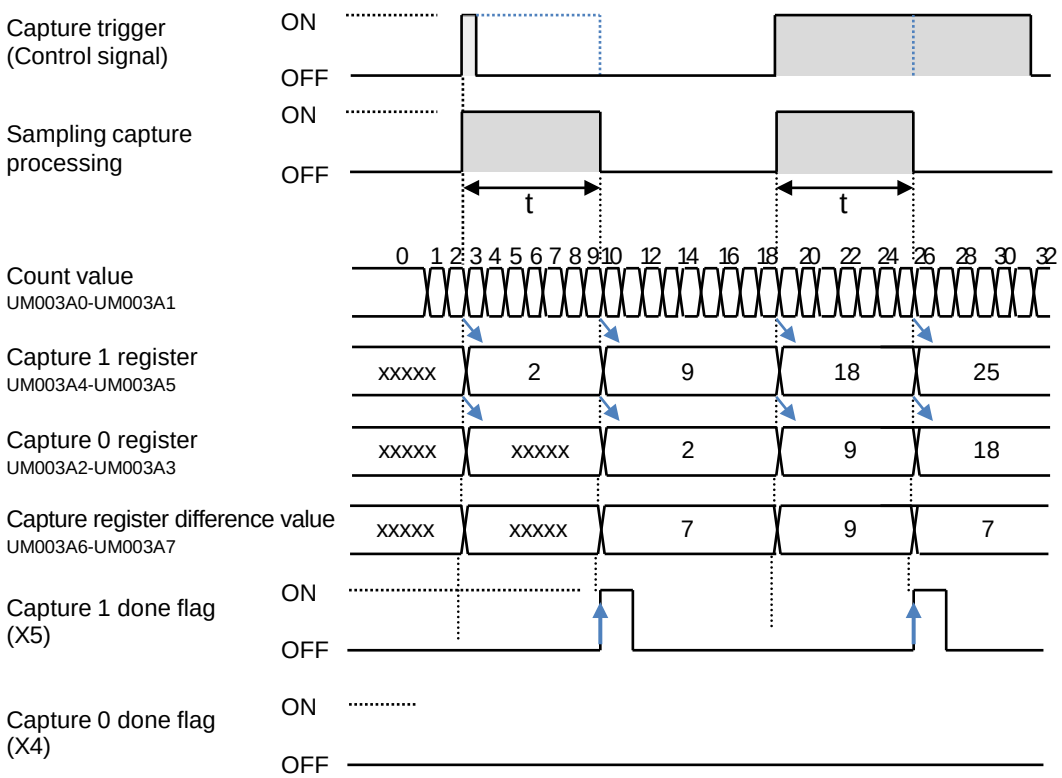
- **The values ((Capture 1 register) - (Capture 0 register)) are always stored as capture register difference values. The signs for the values of capture difference value register change according to the sequence of the capture enable signal (output Y contact) and the capture trigger (control signal).**
- **In the case of continuous operation, the capture 0 register, capture 1 register and capture difference value register are overwritten every time the capture operation is complete. The buffer function can be also used for reading continuous data.**

8.3 Operations of Sampling Capture Function

8.3.1 One operation

- The count values and the difference values are stored in the capture registers (unit memories UM) after a specified sampling time from the time that the control signal is turned on or off.
- The sampling capture function is always enabled when the control signal is allocated to the sampling capture function in the configuration.
- The control signal (positive logic), control signal (negative logic) or output relays (Y7, Y17, Y27, Y37) can be selected as the trigger condition to start the sampling capture.

■ **Time chart**



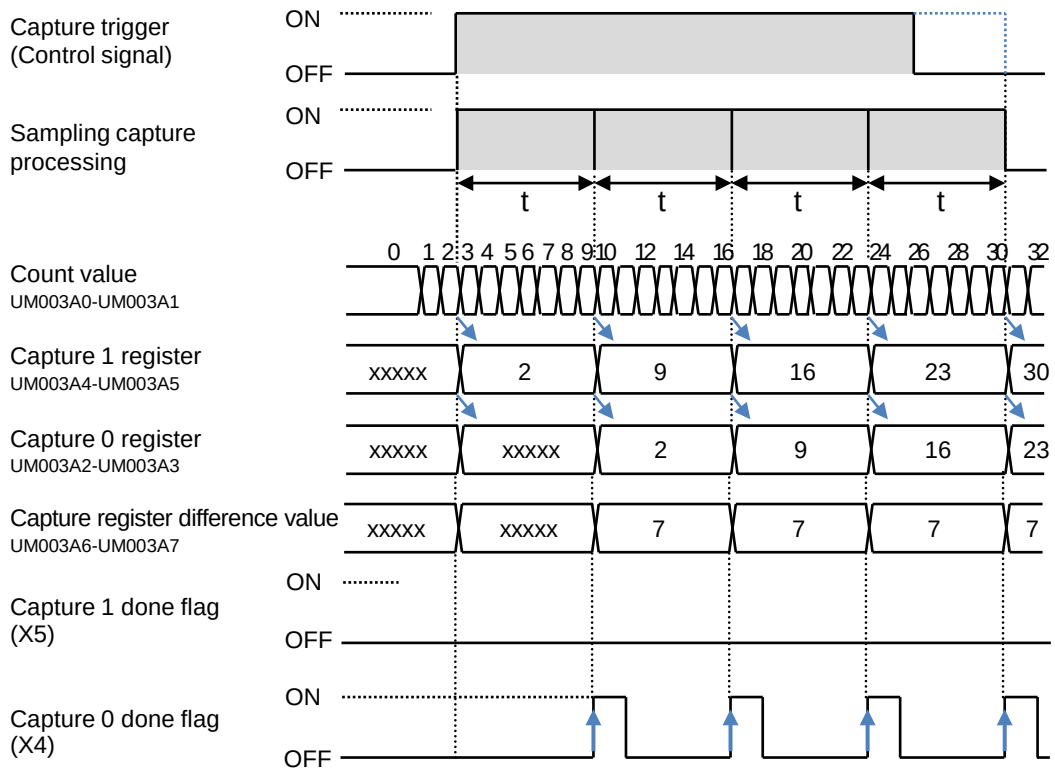
◆ **KEY POINTS**

- **In the sampling capture operation (one operation), the capture 1 done flag is activated. Note that the capture 0 done flag is not activated.**

8.3.2 Continuous Operation

- The count values and the difference values are stored in the capture registers (unit memories UM) continuously at intervals of a specified sampling time after the control signal is turned on or off.
- The sampling capture function is always enabled when the control signal is allocated to the sampling capture function in the configuration.
- The control signal (positive logic), control signal (negative logic) or output relays (Y7, Y17, Y27, Y37) can be selected as the trigger condition to start the sampling capture.

■ **Time chart**



◆ **KEY POINTS**

- **In the sampling capture operation (continuous operation), the capture 0 done flag is activated. Note that the capture 1 done flag is not activated.**

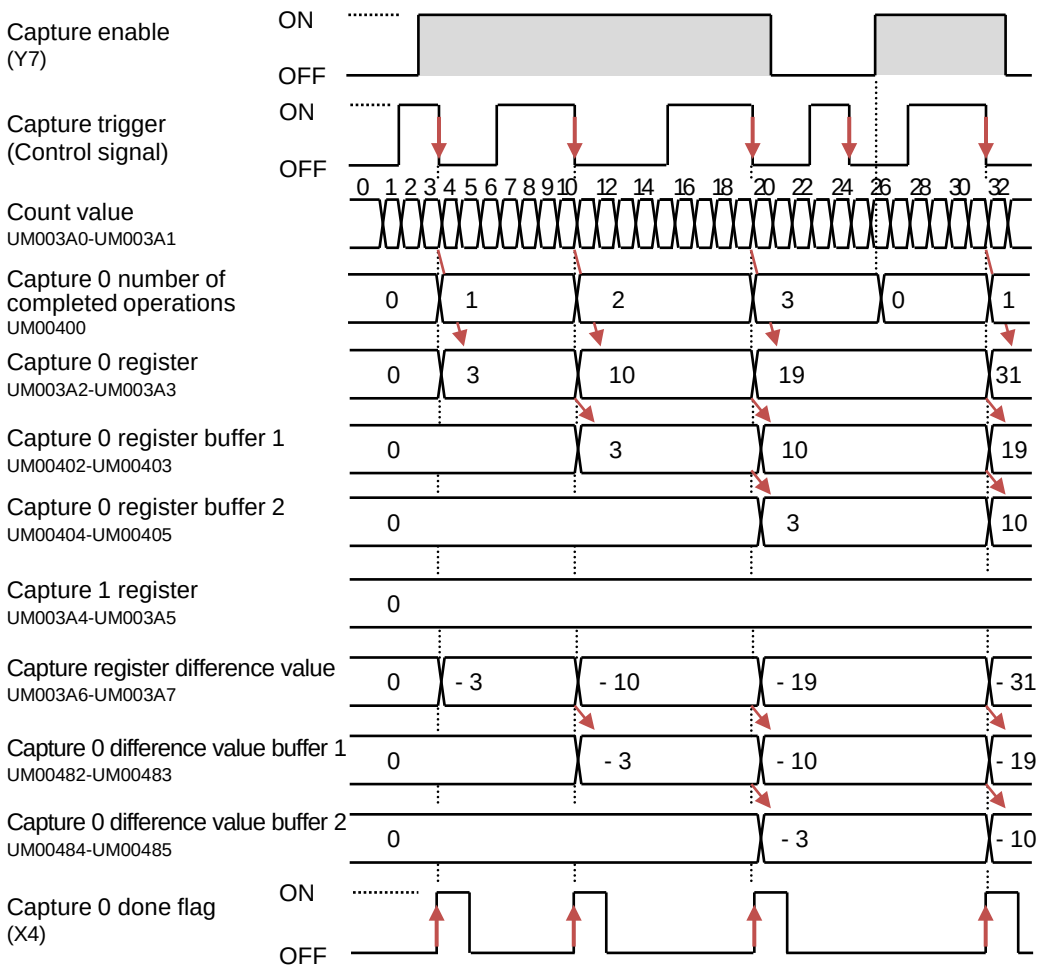
8.4 Operations of Buffer Function

8.4.1 Overview of Buffer Function

■ Function of buffer areas

- In the buffer areas, 60-point (120-word) areas are each provided for the capture 0, capture 1 and difference values each.
- Latest captured data is stored in the capture 0 register or capture 1 register.
- Every time the data in the capture register is updated, the data in the capture register is shifted and stored in the buffer areas 1 to 60 sequentially. The data stored in the buffer 60 (the oldest data) is discarded.

■ Time chart



■ Types of buffer areas

Name	Default	Setting range and description	Unit
Number of completed capture operations	0	Monitors the number of completed capture operations while capturing is enabled. It is reset to zero when the capture request turns on.	-
Capture register buffer (Buffer 1 to Buffer 60)	0	Every time the data in the capture register are updated, the data in the capture register are shifted and stored in sequence. Range:-2,147,483,648 to 2,147,483,647 Signed 32-bit	Pulse
Capture register difference value buffer (Buffer 1 to Buffer 60)	0	Every time the data in the capture register are updated, the data of capture register difference values (Capture 1 register - Capture 0 register) are shifted and stored in sequence. There are two areas, which are for storing data at the time of capture 0 request and the time of capture 1 request. Range: -2,147,483,648 to 2,147,483,647 Signed 32-bit	Pulse

■ Related unit memory (UM) No.

Monitoring item		Unit memory (UM) No.			
		CH0	CH1	CH2	CH3
Capture value buffer area	Number of completed capture 0 operations	UM00400	UM00600	UM00800	UM00A00
	Capture 0 register (Buffer 1 to Buffer 60)	UM00402 - UM00479	UM00602 - UM00679	UM00802 - UM00879	UM00A02 - UM00A79
	Register difference value for capture 0 request (Buffer 1 to Buffer 60)	UM00482 - UM004F9	UM00682 - UM006F9	UM00882 - UM008F9	UM00A82 - UM00AF9
	Number of completed capture 1 operations	UM00500	UM00700	UM00900	UM00B00
	Capture 1 register (Buffer 1 to Buffer 60)	UM00502 - UM00579	UM00702 - UM00779	UM00902 - UM00979	UM00B02 - UM00B79
	Register difference value for capture 1 request (Buffer 1 to Buffer 60)	UM00582 - UM005F9	UM00782 - UM007F9	UM00982 - UM009F9	UM00B82 - UM00BF9

(Note 1) For information on the memory numbers actually used, refer to each items of "11.4 Unit Memory Detailed Specifications". The above list includes empty areas which are reserved in the system. Do not read empty areas or write into empty areas.

8.5 Reading Capture Data

8.5.1 Reading Capture Register Data

■ Area in which capture data is stored

- Latest captured data is stored in the capture 0 register or capture 1 register of unit memory(UM).
- The values ((Capture 1 register) - (Capture 0 register)) are stored in the capture register difference value area.
- They are stored as signed 32-bit data (-2,147,483,648 to 2,147,483,647).

■ Related unit memory (UM) No.

Monitor item		Unit memory (UM) No.			
		CH0	CH1	CH2	CH3
Monitor area	Capture 0 register	UM003A2-UM003A3	UM003B2-UM003B3	UM003C2-UM003C3	UM003D2-UM003D3
	Capture 1 register	UM003A4-UM003A5	UM003B4-UM003B5	UM003C4-UM003C5	UM003D4-UM003D5
	Capture register difference value	UM003A6-UM003A7	UM003B6-UM003B7	UM003C6-UM003C7	UM003D6-UM003D7

■ I/O allocation

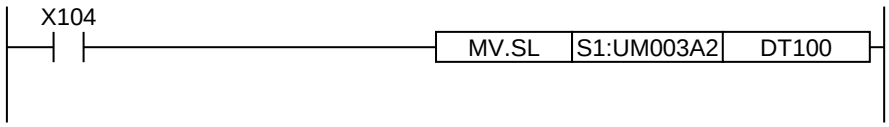
Signal name	CH0	CH1	CH2	CH3
Capture 0 done flag	X104	X124	X144	X164
Capture 1 done flag	X105	X125	X145	X165

(Note 1): The above I/O numbers are those for the slot number 1 and the starting word number 10. The I/O numbers actually used vary according to the slot number where the unit is installed and the starting word number.

■ Sample program

Data is read out to arbitrary operation memories using the done flag which indicates the completion of capture.

Example) Program to read the capture value of CH0 of the high-speed counter unit installed in the slot number 1

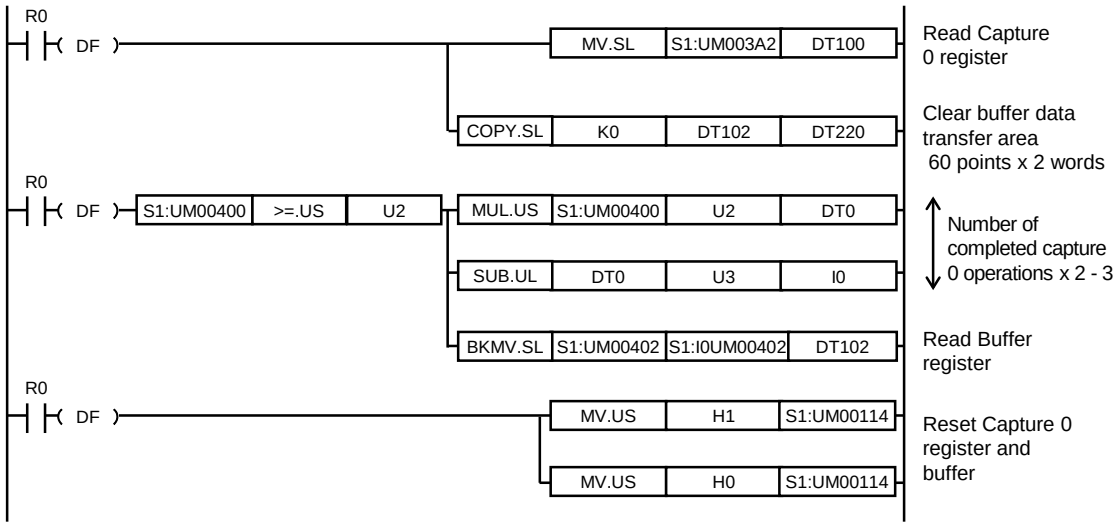


8.5.2 Reading Buffer Area Data

To read data in the buffer area, check the number of completed capture operations (UM00400), and specify the range of the operation memory according to the number.

■ **Sample program**

Example) Program to read the capture value and buffer value of CH0 of the high-speed counter unit installed in the slot number 1



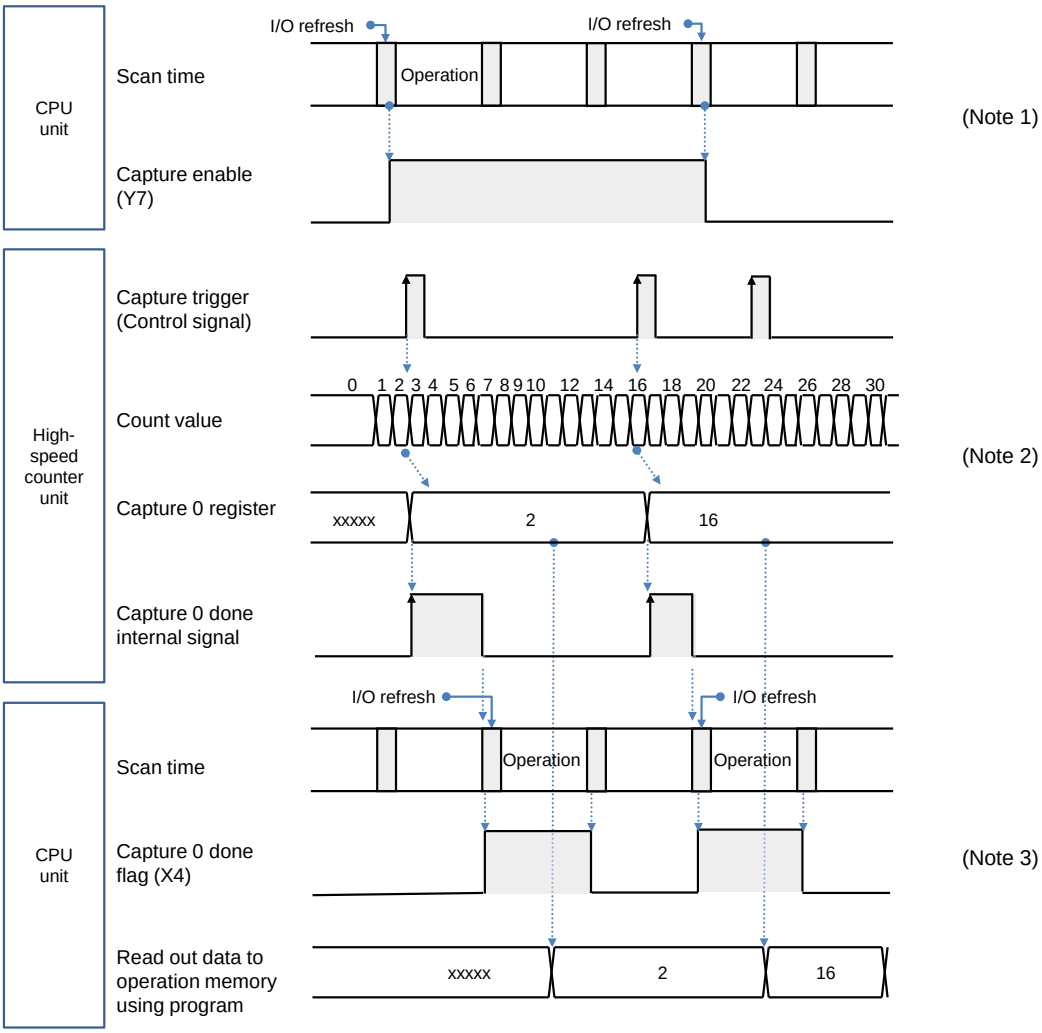
◆ **REFERENCE**

- **For information on the clear of capture registers and buffers, refer to 8.6 Clearing Capture Values Storage Area.**
- **For details of unit memory (UM) numbers, refer to 11.4 Unit Memory Detailed Specifications.**

8.5.3 Operation and Readout of Capture Done Flag (X4/X5)

■ Basic operation

- On the completion of capturing, the capture done flag is reflected in the operation memory of the CPU (X4/X5) at the time of I/O refresh.
- In case of the capture function, the capture done flag is reset by executing the capture enable request signal (Y7).



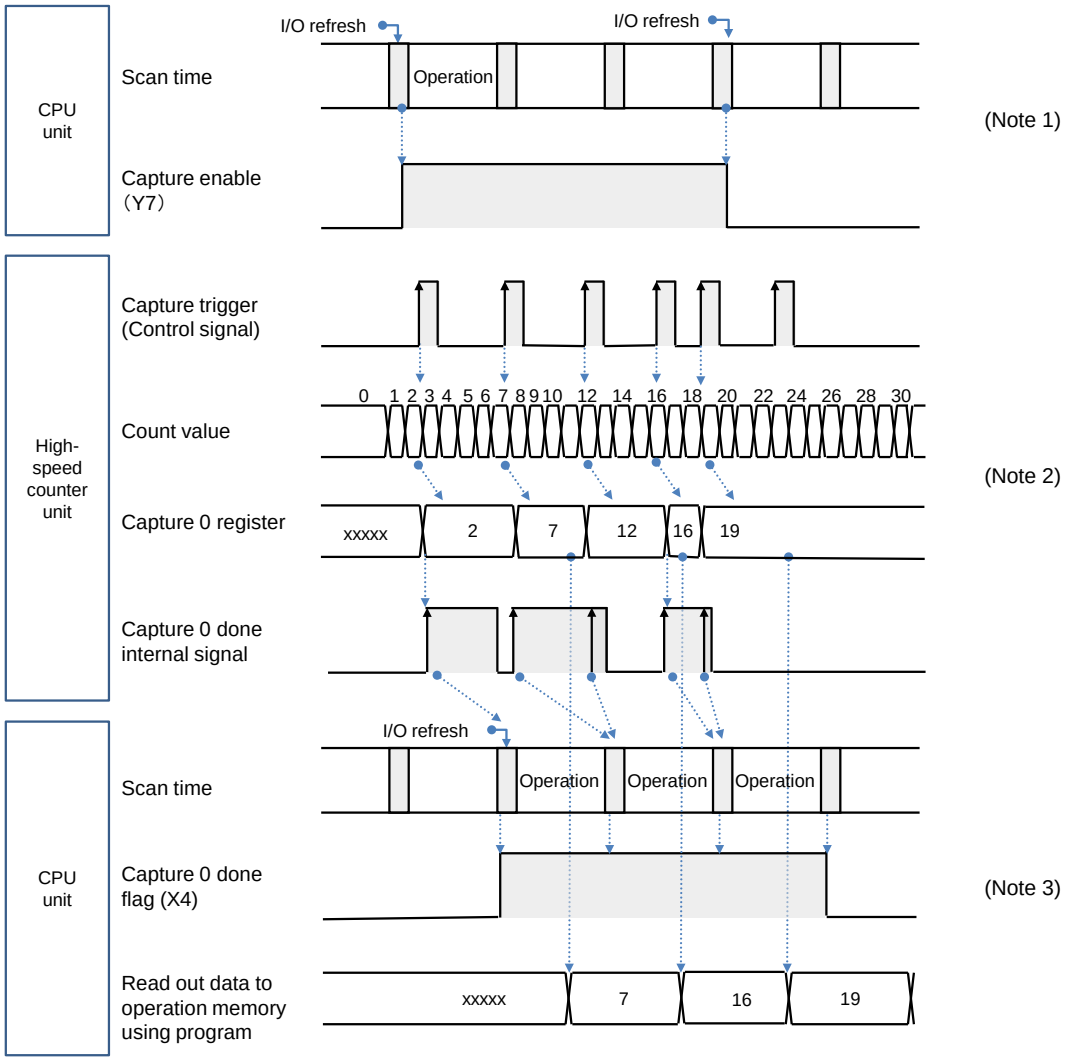
(Note 1) Turn on the capture enable signal using the user program.

(Note 2) The high-speed counter unit performs the capture operation without synchronizing with the operation of the CPU unit every time control signals turn on as the capture trigger. The capture done internal signal used for the system in the high-speed counter unit is reset at the time of I/O refresh of the CPU unit.

(Note 3) The capture done flag of the CPU unit is reflected in the operation memory (X4/X5) at the time of I/O refresh. It is read to an arbitrary operation memory with the user program using the capture done flag. It is read at the timing of an appropriate operation processing.

☛ next page

■ Processing when capture trigger inputs are used frequently



(Note 1) Turn on the capture enable signal using the user program.

(Note 2) The high-speed counter unit performs the capture operation without synchronizing with the operation of the CPU unit every time control signals turn on as the capture trigger. The capture done internal signal used for the system in the high-speed counter unit is reset at the time of I/O refresh of the CPU unit.

(Note 3) The capture done flag of the CPU unit is reflected in the operation memory (X4/X5) at the time of I/O refresh. When multiple capture operations are performed continuously on the high-speed counter unit, the capture done flag (X4/X5) stays ON.

◆ KEY POINTS

- **Whe control signals as capture triggers are input frequently, the capture done flag (X4/X5) stays ON. Note that when reading multiple capture data executed in the high-speed counter unit.**

8.5.4 Reference Information (Manual Reset of Capture Done Flag)

■ Manual reset of capture done flag

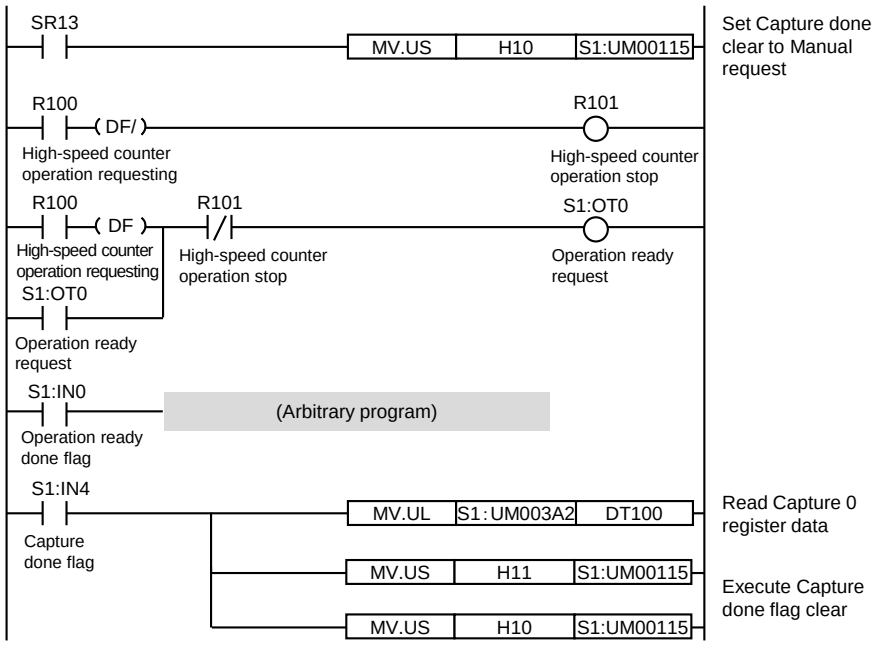
- The capture done flag can also be reset by turning off, on and off the corresponding bit in the capture done flag clear request area.
- The capture 0 done flag and capture 1 done flag can be reset individually.

■ Purpose for manual reset of capture done flag

- For the capture done flag, the operation device direct input (IN) and direct output (OT) are used in combination for confirming if capture operations are completed when performing multiple capture operations in one scan time. When the intervals between capture operations are relatively long compared to the scan time, it is not necessary to use them.

■ Sample program

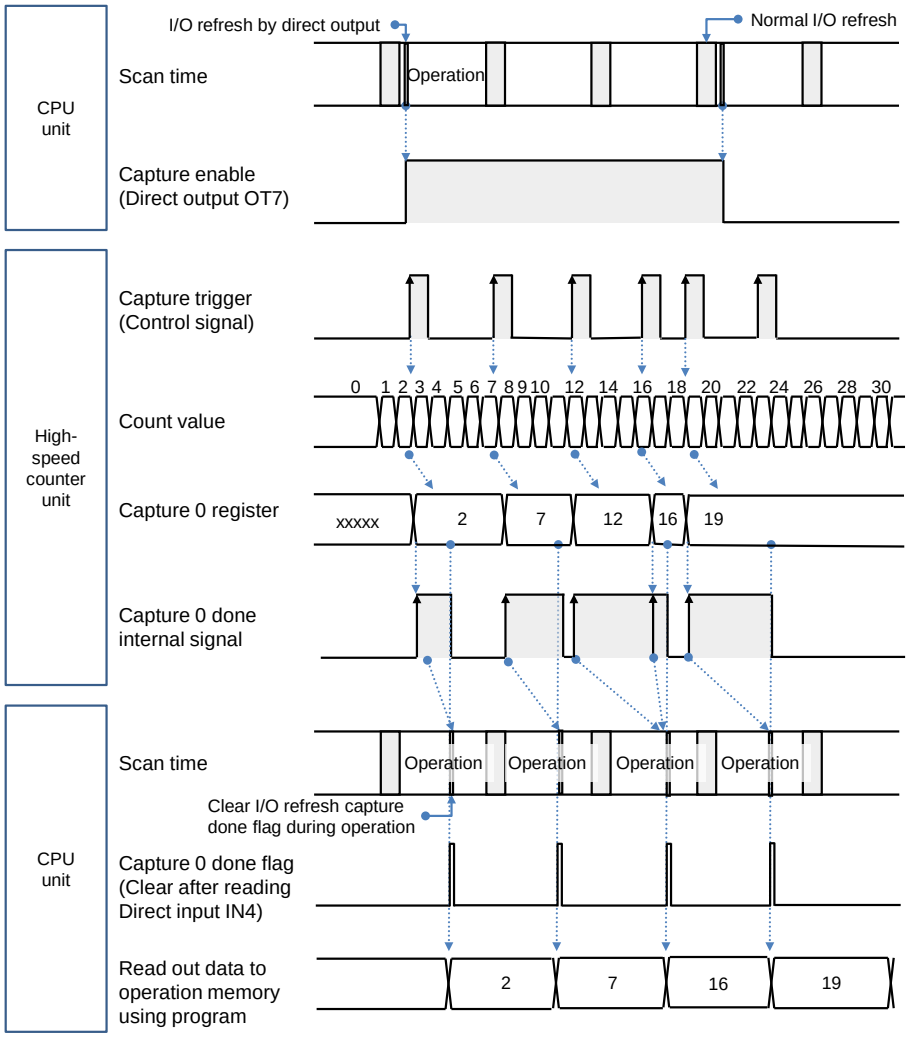
Example) Program to read the capture 0 register of CH0 of the high-speed counter unit installed in the slot No.1 and reset the capture done flag manually



◆ KEY POINTS

- **When using operation devices "Direct input IN" and "Direct output OT", I/O refresh processing is performed during arithmetic processing. For using this operation device, check the box of "Exclude this unit from the scope of I/O refresh" in the I/O map of the FP7 configuration dialog box not to perform the normal I/O refresh process executed in a scan time.**

■ Processing when resetting the capture done flag manually



(Note 1) Turn on the capture enable signal (OT7) using the user program.

(Note 2) The high-speed counter unit performs the capture operation without synchronizing with the operation of the CPU unit every time control signals turn on as the capture trigger. The capture done internal signal used for the system in the high-speed counter unit is reset by the capture done flag clear request.

(Note 3) When reading the capture done flag in the CPU unit with the operation device (IN4/IN5), I/O refresh is performed when executing operation. Also, it is read when corresponding operation processings are performed on user programs. It is read out to arbitrary operation memories.

8.6 Clearing Capture Values Storage Area

8.6.1 Capture Value Clear Request

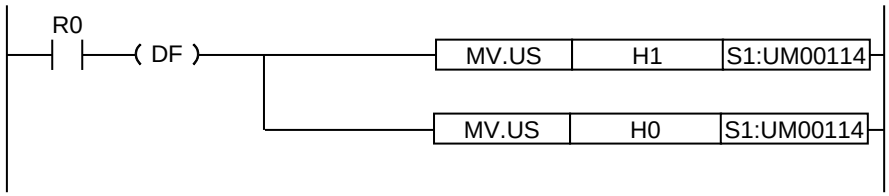
■ **Clearing capture data**

- Capture data can be reset by turning off, on, and off the corresponding bit in the capture value clear request area.
- The capture 0 register and capture 1 register can be reset individually.
- Data stored in the areas of capture registers and capture register buffers is reset to 0 when executing the clear request.

8.6.2 Sample Program

■ **Reset program**

Example) Program to reset the capture 0 register of CH0 of the high-speed counter unit installed in the slot No. 1



◆ **KEY POINTS**

- **Even if the capture value clear request is executed, the number of completed capture operations in the buffer area will not be cleared. The number of completed capture operations will be cleared when the capture enable request (Y7) or the sampling capture function is activated.**

◆ **REFERENCE**

For details of unit memory (UM) numbers, refer to 11.4 Unit Memory Detailed Specifications.

9

Interrupt Program Activation Function

9.1 Interrupt Program Activation Function

9.1.1 Overview of Interrupt Program

- The high-speed counter unit can activate interrupt programs of CPU using comparison match flags.
- If the activation condition is met, the interrupt program of a corresponding program number will be activated. Once the execution of the interrupt program is complete, the process returns to the execution of the main program.

■ **Interrupt program specifications**

Item	Description	
Interrupt program activation condition	Activates a corresponding interrupt program when the comparison match 0 flag and comparison match 1 flag of each channel turns on.	
No. of interrupt programs	Per 1 channel of high-speed counter unit	Max. 2 programs
	Per 1 high-speed counter unit	Max. 4 programs (2-ch type High-speed counter unit) Max. 8 programs (4-ch type High-speed counter unit)
	Per 1 CPU unit	Max. 64 programs (8 programs x 8 units)

9.1.2 Settings of High-speed Counter Unit

■ **Switch setting of the unit**

For using the interrupt program activation function, it is necessary to set the switch on the side of the unit. Refer to “2.1 Names and Functions of Parts”.

■ **Configuration setting**

Confirm if the comparison function has been set and the interrupt function has been set to "Enable" in the configuration menu.

9.1.3 Overview of Interrupt Program

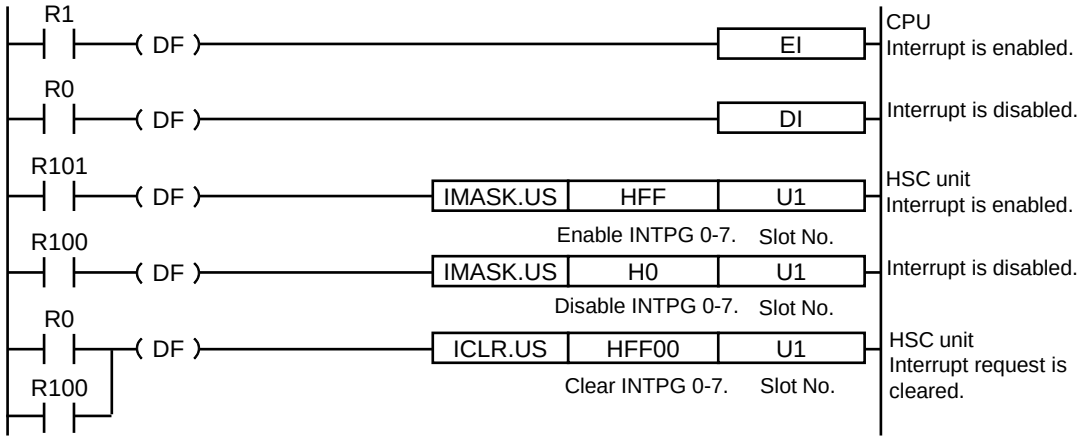
Use the following instructions to execute the interrupt program activation function.

■ **Instructions used for interrupt program activation.**

Described area	Instruction	Function
Main program	EI	Allows the interrupt process for the CPU.
	DI	Prohibits the interrupt process for the CPU.
	IMASK	Allows or prohibits the interrupt process of each unit.
	ICLR	Clears the interrupt activation request signal that has not been processed on the unit side when the interrupt program activation is prohibited by DI or IMASK instruction.
Interrupt program	INTPG	It is described at the beginning of the interrupt program.
	IRET	It is described at the end of the interrupt program.

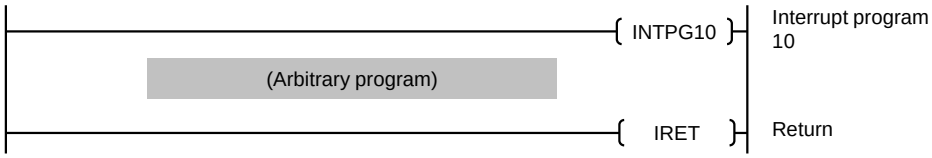
■ Programming method (Main program)

The interrupt for the CPU and the interrupt activation of the high-speed counter unit are allowed in the main program. If the interrupt becomes disabled, clear the interrupt activation request signal that is not processed in the unit as necessary.



■ Programming method (Interrupt program)

- Describe the program to be executed at the time of interrupt process in the interrupt program.



■ Corresponding interrupt program number

Interrupt program No.	Comparison match flag of high-speed counter unit	Designation of the first operand of IMASK and ICLR instructions
INTPG 10	CH0 Comparison match 0 flag	IMASK instruction bit no. 15 … 8 7 … 0 0 0 0 0 0 0 0 0 Higher 8 bits 0: Fixed INTPG 7 ⋮ INTPG 0 0: Disable 1: Enable ICLR instruction bit no. 15 … 8 7 … 0 1 1 1 1 1 1 1 1 Higher 8 bits 1: Fixed INTPG 7 ⋮ INTPG 0 0: Clear 1: Not clear
INTPG 11	CH0 Comparison match 1 flag	
INTPG 12	CH1 Comparison match 0 flag	
INTPG 13	CH1 Comparison match 1 flag	
INTPG 14	CH2 Comparison match 0 flag	
INTPG 15	CH2 Comparison match 1 flag	
INTPG 16	CH3 Comparison match 0 flag	
INTPG 17	CH3 Comparison match 1 flag	

(Note 1): Interrupt program numbers are specified with slot numbers + (0 to 7).The numbers in the above table are for the slot 1.
Example) The interrupt program number corresponding to the CH1 comparison match 1 flag of the slot number 1 is INTPG103.

9.1.4 Precautions for Use

■ **Process when more than one interrupt activation request is made**

- If more than one interrupt activation request is made from the unit, the process will be carried out from the smallest slot number or the smallest interrupt program number.
- If the interrupt activation is requested on the completion of the process of interrupt program, a higher-priority program will be searched and the corresponding interrupt program will be executed.
- Interrupt activation request signals on the unit side will be held until the corresponding interrupt program is executed or ICLR instruction is executed.

◆ NOTE

- **If interrupt occurs many times in one scan, the execution of interrupt program has priority, and the scan time will be longer.**

10

What to Do If an Error Occurs

10.1 Self-diagnostic Function

10.1.1 Errors Announced by High-speed Counter Unit

■ Operation monitor LEDs of high-speed counter

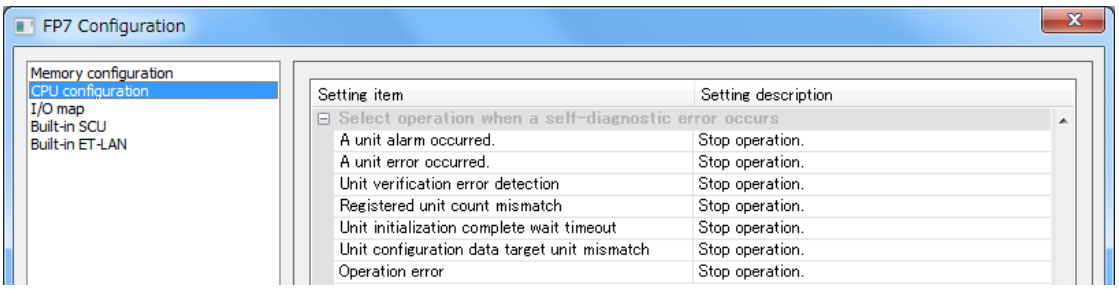
- When an error occurs in the high-speed counter unit, the ERR LED of the unit lights.
- The contents of errors can be confirmed from the error flags and error codes allocated to each channel.
- There are errors which occur at the time of start-up and errors which occur during operations.

■ CPU operation when an error occurs in the high-speed counter unit

- If an error occurs in the high-speed counter unit, it will give the information to the CPU as "Unit error".
- If a "Unit error" occurs, the CPU will stop the operation.
- In the programming tool, the error code (81) unit error is displayed.

■ Operation mode of the CPU when a unit error occurs

- The operation mode of the CPU at the time a unit error occurs can be changed using the configuration menu of programming tool FPWIN GR7.



10.1.2 Confirming Error Code

■ Confirmation of error information

- Error codes are stored in unit memories (UM) for each channel.
- Error codes are read by the device monitor function of programming tool FPWIN GR7.

■ Allocation of I/O signals and unit memories

Signal name	CH0	CH1	CH2	CH3
Overflow annunciation	X10D	X12D	X14D	X16D
Underflow annunciation	X10E	X12E	X14E	X16E
Error annunciation	X10F	X12F	X14F	X16F
Error code storage area	UM00025	UM00026	UM00027	UM00028

(Note 1): The above I/O numbers are those for the slot number 1 and the starting word number 10. The I/O numbers actually used vary according to the slot number where the unit is installed and the starting word number.

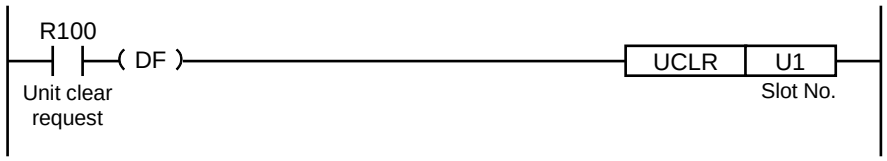
10.1.3 Clearing Errors Using User Programs

- Each error can be cleared by user programs.
- Refer to error codes, correct error factors, and clears the errors.

■ Clearing all channels by UCLR instruction

- Executing the dedicated instruction UCLR (error) clears errors occurred in the high-speed counter unit.

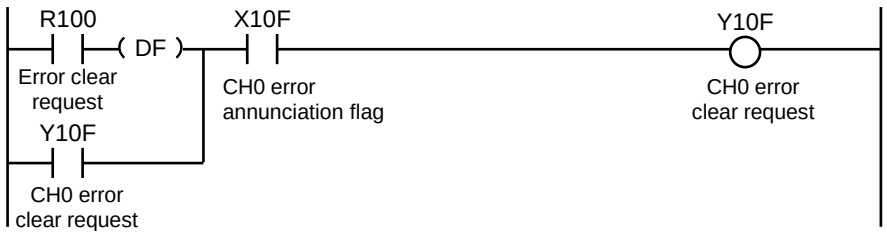
Example) Program to clear errors of the high-speed counter unit installed in the slot No. 1



■ Clearing each channel separately by I/O signals

- Turning on the error clear request flag allocated to the I/O area clears errors in each channel separately. The program below shows the error clear of channel 0.
- The overflow or underflow annunciation flag can be cleared by each clear signal, reset or preset operation. However, error states are not cleared.

Example) Program to request for clearing errors of CH0 of the high-speed counter unit installed in the slot No. 1



■ Allocation of I/O signals

Signal name	CH0	CH1	CH2	CH3
Overflow clear	Y10D	Y11D	Y12D	Y13D
Underflow clear	Y10E	Y11E	Y12E	Y13E
Error clear	Y10F	Y11F	Y12F	Y13F
Overflow annunciation	X10D	X12D	X14D	X16D
Underflow annunciation	X10E	X12E	X14E	X16E
Error annunciation	X10F	X12F	X14F	X16F

(Note 1): The above I/O numbers are those for the slot number 1 and the starting word number 10. The I/O numbers actually used vary according to the slot number where the unit is installed and the starting word number.

10.2 List of Error Codes

10.2.1 Errors in Operation Ready Request (0100H to 0633H)

- These are errors occurred when the operation ready is requested. If these errors occur, the unit will not be ready for operations and the functions set in the unit will not be activated.
- Check if the setting values in the configuration menu or unit memories (UM) are correct.

■ **List of error codes (0100H ~ 0153H)**

Error code	Channel No.	Error name		Corresponding unit memory No.
0100H	CH0	Counter type setting error		UM 00050
0101H	CH1			UM 00120
0102H	CH2			UM 001F0
0103H	CH3			UM 002C0
0110H	CH0	Enable/Disable Overflow/underflow setting error		UM 00051
0111H	CH1			UM 00121
0112H	CH2			UM 001F1
0113H	CH3			UM 002C1
0120H	CH0	Counter upper and lower limits setting error	Upper limit	UM 00052-UM 00053
			Lower limit	UM 00054-UM 00055
0121H	CH1		Upper limit	UM 00122-UM 00123
			Lower limit	UM 00124-UM 00125
0122H	CH2		Upper limit	UM 001F2-UM 001F3
			Lower limit	UM 001F4-UM 001F5
0123H	CH3		Upper limit	UM 002C2-UM 002C3
			Lower limit	UM 002C4-UM 002C5
0130H	CH0	Count direction setting error		UM 00056
0131H	CH1			UM 00126
0132H	CH2			UM 001F6
0133H	CH3			UM 002C6
0140H	CH0	Count input setting error		UM 00057
0141H	CH1			UM 00127
0142H	CH2			UM 001F7
0143H	CH3			UM 002C7
0150H	CH0	Count method setting error		UM 00058
0151H	CH1			UM 00128
0152H	CH2			UM 001F8
0153H	CH3			UM 002C8

■ **List of error codes (0160H ~ 0313H)**

Error code	Channel No.	Error name	Corresponding unit memory No.
0160H	CH0	Input Z signal function setting error	UM 00059
0161H	CH1		UM 00129
0162H	CH2		UM 001F9
0163H	CH3		UM 002C9
0170H	CH0	Control 0 signal function setting error	UM 0005A
0171H	CH1		UM 0012A
0172H	CH2		UM 001FA
0173H	CH3		UM 002CA
0180H	CH0	Control 1 signal function setting error	UM 0005B
0181H	CH1		UM 0012B
0182H	CH2		UM 001FB
0183H	CH3		UM 002CB
0190H	CH0	Default value setting error	UM 00060-UM 00061
0191H	CH1		UM 00130-UM 00131
0192H	CH2		UM 00200-UM 00201
0193H	CH3		UM 002D0-UM 002D1
01A0H	CH0	Input A signal/Input B signal input time constant setting error	UM 00068
01A1H	CH1		UM 00138
01A2H	CH2		UM 00208
01A3H	CH3		UM 002D8
01B0H	CH0	Input Z signal input time constant setting error	UM 00069
01B1H	CH1		UM 00139
01B2H	CH2		UM 00209
01B3H	CH3		UM 002D9
01C0H	CH0	Control signal input time constant setting error	UM 0006A
01C1H	CH1		UM 0013A
01C2H	CH2		UM 0020A
01C3H	CH3		UM 002DA
0300H	CH0	Measurement function selection setting error	UM 00070
0301H	CH1		UM 00140
0302H	CH2		UM 00210
0303H	CH3		UM 002E0
0310H	CH0	Pulse number per rotation setting error	UM 00071-UM 00072
0311H	CH1		UM 00141-UM 00142
0312H	CH2		UM 00211-UM 00212
0313H	CH3		UM 002E1-UM 002E2

■ **List of error codes (0320H ~ 0533H)**

Error code	Channel No.	Error name	Corresponding unit memory No.
0320H	CH0	Average number of frequency measurement processes setting error	UM 00073
0321H	CH1		UM 00143
0322H	CH2		UM 00213
0323H	CH3		UM 002E3
0330H	CH0	Average number of rotation speed measurement processes setting error	UM 00074
0331H	CH1		UM 00144
0332H	CH2		UM 00214
0333H	CH3		UM 002E4
0400H	CH0	Comparison function selection setting error	UM 00078
0401H	CH1		UM 00148
0402H	CH2		UM 00218
0403H	CH3		UM 002E8
0410H	CH0	Comparison input selection setting error	UM 00079
0411H	CH1		UM 00149
0412H	CH2		UM 00219
0413H	CH3		UM 002E9
0430H	CH0	Number of comparison data setting error	UM 0007B
0431H	CH1		UM 0014B
0432H	CH2		UM 0021B
0433H	CH3		UM 002EB
0500H	CH0	External output 0 signal setting error	UM 00100
0501H	CH1		UM 001D0
0502H	CH2		UM 002A0
0503H	CH3		UM 00370
0510H	CH0	External output 0 signal output hold setting error	UM 00101
0511H	CH1		UM 001D1
0512H	CH2		UM 002A1
0513H	CH3		UM 00371
0520H	CH0	External output 0 signal ON timing delay setting error	UM 00102
0521H	CH1		UM 001D2
0522H	CH2		UM 002A2
0523H	CH3		UM 00372
0530H	CH0	External output 0 signal ON hold time setting error	UM 00103
0531H	CH1		UM 001D3
0532H	CH2		UM 002A3
0533H	CH3		UM 00373

■ **List of error codes (0540H ~ 0633H)**

Error code	Channel No.	Error name	Corresponding unit memory No.
0540H	CH0	External output 1 signal setting error	UM 00104
0541H	CH1		UM 001D4
0542H	CH2		UM 002A4
0543H	CH3		UM 00374
0550H	CH0	External output 1 signal output hold setting error	UM 00105
0551H	CH1		UM 001D5
0552H	CH2		UM 002A5
0553H	CH3		UM 00375
0560H	CH0	External output 1 signal ON timing delay setting error	UM 00106
0561H	CH1		UM 001D6
0562H	CH2		UM 002A6
0563H	CH3		UM 00376
0570H	CH0	External output 1 signal ON hold time setting error	UM 00107
0571H	CH1		UM 001D7
0572H	CH2		UM 002A7
0573H	CH3		UM 00377
0600H	CH0	Capture 0 setting error	UM 00110
0601H	CH1		UM 001E0
0602H	CH2		UM 002B0
0603H	CH3		UM 00380
0610H	CH0	Capture 1 setting error	UM 00111
0611H	CH1		UM 001E1
0612H	CH2		UM 002B1
0613H	CH3		UM 00381
0620H	CH0	Sampling capture function operation setting error	UM 00112
0621H	CH1		UM 001E2
0622H	CH2		UM 002B2
0623H	CH3		UM 00382
0630H	CH0	Sampling time setting error	UM 00113
0631H	CH1		UM 001E3
0632H	CH2		UM 002B3
0633H	CH3		UM 00383

10.2.2 Errors Occurred in Operations (1000H to 1043H)

- These are errors occurred in operations.
- Take steps according to the contents in the table below.

■ **List of error codes**

Error code	Channel No.	Error name	Content	Operation	Countermeasures
1000H	CH0	Overflow error	The count value exceeds the upper limit.	Announces the overflow error. Holds the count value.	Performs the reset or preset operation to make the count value be in the range of upper and lower limits.
1001H	CH1				
1002H	CH2				
1003H	CH3				
1010H	CH0	Underflow error	The count value exceeds the lower limit.	Announces the underflow error. Holds the count value.	Performs the reset or preset operation to make the count value be in the range of upper and lower limits.
1011H	CH1				
1012H	CH2				
1013H	CH3				
1020H	CH0	Reset error	The count value becomes 0 under the reset condition, and it is outside the range of upper and lower limits.	Does not reset. Continues the count operation.	Confirm the settings of the upper and lower limits of counter. If 0 does not exist in the range of the upper and lower limits, make the preset request.
1021H	CH1				
1022H	CH2				
1023H	CH3				
1030H	CH0	Preset error	The count value is outside the range of upper and lower limits under the preset condition.	Does not preset. Continues the count operation.	Confirm if the specified preset value is in the range of upper and lower limits.
1031H	CH1				
1032H	CH2				
1033H	CH3				
1040H	CH0	Current value change error	The count value is outside the range of upper and lower limits when the current value is changed.	Does not change the current value. Continues the count operation.	Confirm if the current value changed value is in the range of upper and lower limits.
1041H	CH1				
1042H	CH2				
1043H	CH3				

11
Specifications

11.1 Specifications

11.1.1 General Specifications

Items	Description
Operating ambient temperature	0°C to +55°C
Storage ambient temperature	-40°C to +70°C
Operating ambient humidity	10% to 95%RH (at 25°C with no-condensing)
Storage ambient humidity	10% to 95%RH (at 25°C with no-condensing)
Breakdown voltage	Between I/O terminals and CPU power supply terminal/function earth Bewteen input terminal and output terminals 500 VAC for 1 min. (Cutoff current: 10 mA, factory default setting)
Insulation resistance	Between I/O terminals and CPU power supply terminal/function earth Bewteen input terminal and output terminals 100 MΩ or more (with 500 VDC megohmmeter)
Vibration resistance	Conforming to JISB3502 and IEC61131-2. 5 to 8.4 Hz, 3.5-mm single amplitude 8.4 to 150 Hz, acceleration of 9.8 m/s2 10 sweeps each in X, Y, and Z directions (1 octave/min)
Shock resistance	Conforming to JISB3502 and IEC61131-2. 147 m/s^2 or more in X, Y, and Z directions three times each
Noise resistance	1,000 V [P-P] with pulse width of 1 μs or 50 ns (based on in-house measurements)
Environment	Free from corrosive gases and excessive dust
EU Directive applicable standard	EMC Directive: EN61131-2
Overvoltage category	Category II
Pollution degree	Pollution level 2
Internal current consumption	65 mA or less
Weight	Approx. 130 g

11.1.2 Function Specifications

Items		Description	
Count function	Product No.	AFP7HSC2T	AFP7HSC4T
	No. of counters	2-ch type	4-ch type
	Counter type	Linear counter, Ring counter	
	Counting range	Signed 32-bit (-2,147,483,648 to +2,147,483,647)	
	Max. input frequency	4MHz/8MHz for individual input (phases A and B) (Duty ratio 50±10%) 4MHz/8MHz for direction detection input (Duty ratio 50%±10%) 4MHz/8MHz for 2-phase input (Duty ratio 50±10%, Phase shifting below 5%)	
	Input signal	Phases A, B and Z	
	External I/O	- Control signal input: 4 points (2 points/ch) - External output: 4 points (2 points/ch)	- Control signal input: 8 points (2 points/ch) - External output: 8 points (2 points/ch)
	Input type	- 2-phase input (Phase difference input) 1 multiple, 2 multiple, 4 multiple - Individual input 1 multiple, 2 multiple - Direction detection input 1 multiple, 2 multiple	
	Count operation function	Count operation can be controlled by input signals in combination with three functions. - Counter enable function (Control signal/Output Y relay) - Preset function (Input Z signal/Output Y relay) - Preset function (Input Z signal/Output Y relay) Only for control signals, the enable function and reset function or preset function can be combined. The count operation is set by selecting from the following operations. - Reset operation at rising edge - Reset operation at trailing edge - Positive logic reset operation - Negative logic reset operation - Preset operation at rising edge - Preset operation at trailing edge - Positive logic preset operation - Negative logic preset operation - Positive logic enable operation - Negative logic enable operation - Positive logic enable operation and reset operation at rising edge - Negative logic enable operation and reset operation at trailing edge - Positive logic enable operation and preset operation at rising edge - Negative logic enable operation and preset operation at trailing edge	
Measurement function	Frequency measurement function	Measures the intervals between the changes in the count value, and calculates the frequency.	
	Rotation speed measurement A function	Measures the intervals between the changes in the count value, and automatically calculates the rotation speed.	
	Rotation speed measurement B function	Measures the time for the number of counts equivalent to one rotation. Sets the time to reach the specified number of pulses per one rotation, and calcualtes the rotation speed from the time required for one rotation.	

Items		Description	
Comparison function	No. of comparison data	Max. 16 data/ch (Comparison data 0 to Comparison data 15)	
	Comparison match flag	Max. 16 points/ch (Comparison match 0 flag to Comparison match F flag) Read as input relays (X) by user programs. Multiple comparison match flags can be set for one comparison data.	
	Target value match function	Depending on the count direction, sets or resets the output when the count value reaches the target value.	
	Band comparison function	Turns on/off the output when the count value reaches the area of the target value.	
External output function	No. of external outputs	2 points/ch Comparison match 0 flag and comparison match 1 flag can be allocated to external outputs.	
	Comparison result output function	When using the band comparison function, the ON timing characteristics of external output relays can be changed. ON timing delay ON hold time ON timing delay and ON hold time	
	Forced output function	Outpus can be forcibly set or reset by the monitor function of programming tool.	
Other functions	Capture function	Stores the count value when the control signal turns on in the capture register. Either one of the following functions is usable.	
		Capture function	Max. 2 points Stores the count value when the capture trigger turns on in the capture register.
		Sampling capture function	Max. 1 point Stores the count values for a specified sampling time when the capture trigger turns on in the capture register.
	Interrupt function	Activates corresponding interrupt programs when the comparison match 0 flag and comparison match 1 flag of each channel turns on. (Note 1) (Note 2)	
		Per 1 channel of high-speed counter unit	Max. 2 programs
		Per 1 high-speed counter unit	Max. 4 programs (2-ch type High-speed counter unit), Max. 8 programs (4-ch type High-speed counter unit)
		Per 1 CPU unit	Max. 64 programs (8 programs x 8 units)
	Initial value of counter	The count value overwrites the initial value when the power turns on.	
	Input time constant	Input time constant (noise filter) can be set to reduce noises of input signal lines.	
		Input A signal, input B signal (The same time constant for the both signals)	0.1 μs (2 MHz), 0.2 μs (1 MHz), 0.5 μs(500 kHz), 1.0 μs (250 kHz), 2.0 μs (100 kHz), 10.0 μs (10 kHz)
		Input Z signal	0.1 μs (2 MHz), 0.2 μs (1 MHz), 0.5 μs (500 kHz), 1.0 μs (250 kHz), 2.0 μs (100 kHz), 10.0 μs (10 kHz)
		Control signal	2 μs, 5 μs, 10 μs, 20 μs, 50 μs, 100 μs, 500 μs, 1 ms, 2 ms, 5 ms, 10ms

(Note 1) If interrupt occurs many times in one scan, the execution of intterupt program has priority, and the scan time will be longer.

(Note 2) If more than one interrupt activation request is made from the unit, the process will be carried out from the smallest slot number or the smallest interrupt program number.

11.2 Allocation of I/O Numbers

■ **Input relays**

I/O number								Name	Description
CH0		CH1		CH2		CH3			
WX0	X0	WX2	X20	WX4	X40	WX6	X60	Operation ready done	Flag to indicate the counter operation is ready.
	X1		X21		X41		X61	Counter enable	Flag to indicate the counter operation is enabled.
	X2		X22		X42		X62	Count direction	Flag to indicate a count direction. ON: Forward (Addition) OFF: Reverse (Subtraction)
	X3		X23		X43		X63	—	—
	X4		X24		X44		X64	Capture 0 done flag	Flag to announce that the count value is stored in capture 0 register.
	X5		X25		X45		X65	Capture 1 done flag	Flag to announce that the count value is stored in capture 1 register.
	X6		X26		X46		X66	External output 0 signal monitor	Monitors the output state of external output 0 signal.
	X7		X27		X47		X67	External output 1 signal monitor	Monitors the output state of external output 1 signal.
	X8		X28		X48		X68	Input A signal monitor	Monitors the input state of input A signal.
	X9		X29		X49		X69	Input B signal monitor	Monitors the input state of input B signal.
	XA		X2A		X4A		X6A	Input Z signal monitor	Monitors the input state of input Z signal.
	XB		X2B		X4B		X6B	Control 0 signal monitor	Monitors the output state of control 0 signal.
	XC		X2C		X4C		X6C	Control 1 signal monitor	Monitors the output state of control 1 signal.
	XD		X2D		X4D		X6D	Overflow annunciation	Flag to announce the occurrence of overflow (Enabled for the linear counter only.)
	XE		X2E		X4E		X6E	Underflow annunciation	Flag to announce the occurrence of underflow (Enabled for the linear counter only.)
	XF		X2F		X4F		X6F	Error annunciation	Flag to announce the occurrence of an error.
WX1	X10 ~ X19	WX3	X30 ~ X39	WX5	X50 ~ X59	WX7	X70 ~ X79	Comparison match 0 flag to Comparison match 9 flag	Flag to reflect the results of the band comparison function or target value match function.
	X1A ~ X1F		X3A ~ X3F		X5A ~ X5F		X7A ~ X7F	Comparison match A flag to Comparison match F flag	

(Note 1): The I/O numbers actually allocated are the numbers based on the starting word number allocated to the unit.
Example) When the starting word number for the unit is "10", the operation ready done flag for CH0 is X100.

■ **Output relays**

I/O number								Name	Effective condition	Description
CH0		CH1		CH2		CH3				
WY0	Y0	WY1	Y10	WY2	Y20	WY3	Y30	Operation ready request	Level	Relay to recalculate the setting parameter of counter.
	Y1		Y11		Y21		Y31	Count enable request	Level	Relay to start the counter operation.
	Y2		Y12		Y22		Y32	Reset request	ON edge	Relay to reset count values.
	Y3		Y13		Y23		Y33	Preset request	ON edge	Relay to preset count values.
	Y4		Y14		Y24		Y34	Reset enable request	Level	Relay to enable the reset by the control signal and input Z signal.
	Y5		Y15		Y25		Y35	Current value change request	ON edge	Relay to request for changing the current value of counter.
	Y6		Y16		Y26		Y36	Preset value change request	ON edge	Relay to request for changing preset values.
	Y7		Y17		Y27		Y37	Capture enable request (Note 2)	Level	Capture enable request when using the capture function or capture trigger signal when using the sampling capture function.
	Y8		Y18		Y28		Y38	—	—	—
	Y9		Y19		Y29		Y39	External output 0 forced ON	Level	Relay to forcibly turn on the external output 0.
	YA		Y1A		Y2A		Y3A	External output 0 forced OFF	Level	Relay to forcibly turn off the external output 0.
	YB		Y1B		Y2B		Y3B	External output 1 forced ON	Level	Relay to forcibly turn on the external output 1.
	YC		Y1C		Y2C		Y3C	External output 1 forced OFF	Level	Relay to forcibly turn off the external output 1.
	YD		Y1D		Y2D		Y3D	Overflow clear	ON edge	Relay to clear the overflow annunciation flag.
	YE		Y1E		Y2E		Y3E	Underflow clear	ON edge	Relay to clear the underflow annunciation flag.
	YF		Y1F		Y2F		Y3F	Error clear	ON edge	Relay to clear errors.

(Note 1): The I/O numbers in the table indicates offset addresses. The I/O numbers actually allocated are the numbers based on the starting word number allocated to the unit.
Example) When the starting word number for the unit is "10", the operation ready request flag for CH0 is Y100.

(Note 2) How the capture enable request signal works varies according to the functions to be used.

11.3 List of Unit Memories

■ **Check list of unit memories**

Setting monitor item		Unit memory (UM) number			
		CH0	CH1	CH2	CH3
Common setting area	Error code	UM 00025	UM 00026	UM 00027	UM 00028
Individual setting area	Count function setting area	UM 00050 - UM 0006F	UM 00120 - UM 0013F	UM 001F0 - UM 0020F	UM 002C0 - UM 002DF
	Measurement function setting area	UM 00070 - UM 00077	UM 00140 - UM 00147	UM 00210 - UM 00217	UM 002E0 - UM 002E7
	Comparison function setting area	UM 00078 - UM 000FF	UM 00148 - UM 001CF	UM 00218 - UM 0029F	UM 002E8 - UM 0036F
	External output function setting area	UM 00100 - UM 0010F	UM 001D0 - UM 001DF	UM 002A0 - UM 002AF	UM 00370 - UM 0037F
	Capture function setting area	UM 00110 - UM 00117	UM 001E0 - UM 001E7	UM 002B0 - UM 002B7	UM 00380 - UM 00387
	Interrupt function setting area	UM00118 - UM0011F	UM001E8 - UM 001EF	UM002B8 - UM 002BF	UM00388 - UM 0038F
Monitor area	Count value	UM003A0 - UM003A1	UM003B0 - UM003B1	UM003C0 - UM003C1	UM003D0 - UM003D1
	Capture 0 register	UM003A2 - UM003A3	UM003B2 - UM003B3	UM003C2 - UM003C3	UM003D2 - UM003D3
	Capture 1 register	UM003A4 - UM003A5	UM003B4 - UM003B5	UM003C4 - UM003C5	UM003D4 - UM003D5
	Capture register difference value	UM003A6 - UM003A7	UM003B6 - UM003B7	UM003C6 - UM003C7	UM003D6 - UM003D7
	Frequency measurement (Averaging)	UM003A8 - UM003A9	UM003B8 - UM003B9	UM003C8 - UM003C9	UM003D8 - UM003D9
	Rotation speed measurement (Averaging)	UM003AA - UM003AB	UM003BA - UM003BB	UM003CA - UM003CB	UM003DA - UM003DB

(Note 1): For information on the memory numbers actually used, refer to each items of "11.4 Unit Memory Detailed Specifications". The above list includes empty areas which are reserved in the system. Do not read empty areas or write into empty areas.

■ Check list of unit memories

Setting monitor item		Unit memory (UM) No.			
		CH0	CH1	CH2	CH3
Capture value buffer area	Number of completed capture 0 operations	UM00400	UM00600	UM00800	UM00A00
	Capture 0 register (Buffer 1 to Buffer 60)	UM00402 - UM00479	UM00602 - UM00679	UM00802 - UM00879	UM00A02 - UM00A79
	Capture 0 register difference value (Buffer 1 to Buffer 60)	UM00482 - UM004F9	UM00682 - UM006F9	UM00882 - UM008F9	UM00A82 - UM00AF9
	Number of completed capture 1 operations	UM00500	UM00700	UM00900	UM00B00
	Capture 1 register (Buffer 1 to Buffer 60)	UM00502 - UM00579	UM00702 - UM00779	UM00902 - UM00979	UM00B02 - UM00B79
	Capture 1 register difference value (Buffer 1 to Buffer 60)	UM00582 - UM005F9	UM00782 - UM007F9	UM00982 - UM009F9	UM00B82 - UM00BF9

(Note 1): For information on the memory numbers actually used, refer to each items of "11.4 Unit Memory Detailed Specifications". The above list includes empty areas which are reserved in the system. Do not read empty areas or write into empty areas.

11.4 Unit Memory Detailed Specifications

11.4.1 Common Setting Area

■ **Error code**

Unit memory No.(Hex)	Name	Default	Setting range and description
UM 00025	ch0 Error code	H0	Stores error code for each channel. Refer to the error code list.
UM 00026	ch1 Error code	H0	
UM 00027	ch2 Error code	H0	
UM 00028	ch3 Error code	H0	

11.4.2 Individual Setting Area

■ **Count function**

Unit memory No.(Hex)	Name	Default	Setting range and description	Unit
UM 00050 UM 00120 UM 001F0 UM 002C0	Counter type	H0	Set the type of counter. H0: Linear counter H1: Ring counter	—
UM 00051 UM 00121 UM 001F1 UM 002C1	Enable/Disable overflow/ underflow	H0	Set whether to enable or disable the overflow/underflow judgement. H0: Disable, H1: Enable Annunciation using overflow and underflow flags of each channel and error codes. However, when it is set to disable, the upper and lower limits are disregarded and counting continues.	—
UM 00052 UM 00053 UM 00122 UM 00123 UM 001F2 UM 001F3 UM 002C2 UM 002C3	Counter upper limit	U 2,147,483,647	Set the upper limit of counter. Setting range: -2,147,483,647 (8000 0001H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit However, the upper limit should be larger than the lower limit. A setting error occurs when the upper limit is equal to the lower limit or smaller than the lower limit.	Pulse
UM 00054 UM 00055 UM 00124 UM 00125 UM 001F4 UM 001F5 UM 002C4 UM 002C5	Counter lower limit	U -2,147,483,648	Set the lower limit of counter. Setting range: -2,147,483,648 (8000 0000H) to 2,147,483,646 (7FFF FFFEH) Signed 32-bit However, the upper limit should be larger than the lower limit. A setting error occurs when the upper limit is equal to the lower limit or smaller than the lower limit.	Pulse

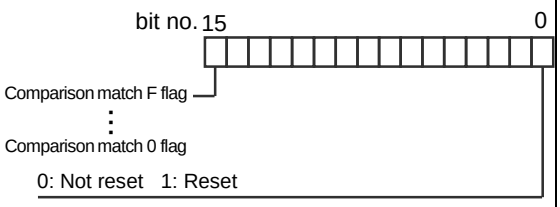
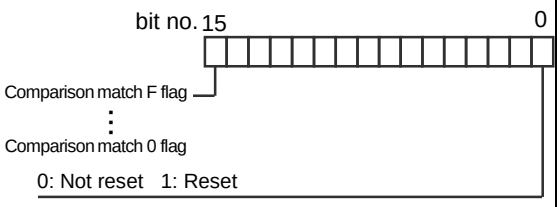
(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

■ Count function

Unit memory No.(Hex)	Name	Default	Setting range and description	Unit
UM 00056 UM 00126 UM 001F6 UM 002C6	Specify count direction	H0	Set the direction of count. H0: Count in normal direction H1: Count in reverse direction	—
UM 00057 UM 00127 UM 001F7 UM 002C7	Select count input	H0	Select a signal for counting from the count signal, internal clock or internal control signal. H0: Count signal H1: Internal clock 0.25 us (4 MHz) H2: Internal clock 1.00 us (1 MHz) H3: Internal clock 10 us (100 kHz) H4: Internal clock 100 us (10 kHz) H7: Internal control signal	—
UM 00058 UM 00128 UM 001F8 UM 002C8	Count method	H0	Set the count method. H0: 2-phase input 1 multiple H1: 2-phase input 2 multiple H2: 2-phase input 4 multiple H3: Individual input 1 multiple H4: Individual input 2 multiple H5: Direction detection input 1 multiple H6: Direction detection input 2 multiple	—
UM 00059 UM 00129 UM 001F9 UM 002C9	Input Z signal function setting	H0	Set counter operations by the input Z signal. H0: Not used H1: Reset operation at rising edge H2: Reset operation at trailing edge H3: Positive logic reset operation H4: Negative logic reset operation H5 : Preset operation at rising edge H6 : Preset operation at trailing edge H7: Positive logic preset operation H8: Negative logic preset operation	—
UM 0005A UM 0012A UM 001FA UM 002CA	Control 0 signal function setting	H0	Set counter operations by the control 0 signal. H0: Not used H1: Positive logic enable operation H2: Negative logic enable operation H3: Positive logic enable operation, reset operation at rising edge H4: Negative logic enable operation and reset operation at trailing edge H5: Positive logic enable operation and preset operation at rising edge H6: Negative logic enable operation and preset operation at trailing edge	—
UM 0005B UM 0012B UM 001FB UM 002CB	Control 1 signal function setting	H0	Set counter operations by the control 1 signal. H0: Not used H1: Positive logic enable operation H2: Negative logic enable operation	—

(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

■ Count function

Unit memory No.(Hex)	Name	Default	Setting range and description	Unit
UM 0005C UM 0012C UM 001FC UM 002CC	Comparison match leading edge reset	H0	Set to reset the counter when the comparison match flag rises. 	—
UM 0005D UM 0012D UM 001FD UM 002CD	Comparison match trailing edge reset	H0	Set to reset the counter when the comparison match flag falls. 	—
UM 00060 UM 00061 UM 00130 UM 00131 UM 00200 UM 00201 UM 002D0 UM 002D1	Default	U0	Set the default value used when the power turns on. Setting range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
UM 00062 UM 00063 UM 00132 UM 00133 UM 00202 UM 00203 UM 002D2 UM 002D3	Preset value	U0	Set the preset value. Setting range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
UM 00064 UM 00065 UM 00134 UM 00135 UM 00204 UM 00205 UM 002D4 UM 002D5	Current value changed value	U0	Set the current value changed value to change the current count value of counter. Setting range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse

(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

■ Count function0

Unit memory No.(Hex)	Name	Default	Setting range and description	Unit
UM 00068 UM 00138 UM 00208 UM 002D8	Input A signal/Input B signal input time constant	H5	Set the input time constants of input A signal and input B signal. H0: No input time constant H1: 0.1 us(2 MHz) H2: 0.2 us(1 MHz) H3: 0.5 us(500 kHz) H4: 1.0 us(250 kHz) H5: 2.0 us(100 kHz) H6:10.0 us(10 kHz) H7: Disable (No input time constant)	—
UM 00069 UM 00139 UM 00209 UM 002D9	Input Z signal input time constant	H5	Set the input time constant of input Z signal. H0: No input time constant H1: 0.1 us(2 MHz) H2: 0.2 us(1 MHz) H3: 0.5 us(500 kHz) H4: 1.0 us(250 kHz) H5: 2.0 us(100 kHz) H6:10.0 us(10 kHz) H7: Disable (No input time constant)	—
UM 0006A UM 0013A UM 0020A UM 002DA	Control signal input time constant	H9	Set the input time constant of control signal. H0: No input time constant H1: 2 us H2: 5 us H3: 10 us H4: 20 us H5: 50 us H6: 100 us H7: 500 us H8: 1.0 ms H9: 2.0 ms HA: 5.0 ms HB: 10.0 ms HC: Disable (No input time constant) HD: Disable (No input time constant) HE: Disable (No input time constant) HF: Disable (No input time constant)	—

(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

■ Measurement function

Unit memory No.(Hex)	Name	Default	Setting range and description	Unit
UM 00070 UM 00140 UM 00210 UM 002E0	Select measurement function	H0	Select a measurement function from frequency measurement, rotation speed measurement A or rotation speed measurement B. H0: Not use measurement function H1: Frequency measurement H2: Frequency measurement and rotation speed measurement A H3: Frequency measurement and rotation speed measurement B	—
UM 00071 UM 00072 UM 00141 UM 00142 UM 00211 UM 00212 UM 002E1 UM 002E2	Pulse number per rotation	U1	Set the pulse number for one rotation of the encoder. Setting range: 1 to 1,048,575 (The values out of the setting range are invalid.)	Pulse
UM 00073 UM 00143 UM 00213 UM 002E3	Set averange number of frequency measurement processes	H0	Set the number of averaging of frequency measurement values. H0: No averaging H1: 2 times H2: 4 times H3: 8 times H4: 16 times H5: 32 times H6: 64 times H7: 128 times	Times
UM 00074 UM 00144 UM 00214 UM 002E4	Set average number of rotation speed measurement processes	H0	Set the number of averaging of rotation speed measurement values. H0: No averaging H1: 2 times H2: 4 times H3: 8 times H4: 16 times H5: 32 times H6: 64 times H7: 128 times	Times

(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

■ Comparison function

Unit memory No.(Hex)	Name	Default	Setting range and description	Unit
UM 00078 UM 00148 UM 00218 UM 002E8	Select comparison function	H0	Select a method of the comparison function from band comparison or target value match comparison. H0: Not use H1: Band comparison H2: Target value match comparison	—
UM 00079 UM 00149 UM 00219 UM 002E9	Select comparison input	H0	Select a target of the comparison function from count value or measurement value. H0: Count value H1: Measurement value (Frequency) H2: Measurement value (Rotation speed)	—
UM 0007B UM 0014B UM 0021B UM 002EB	Set number of comparison data	U16	Set the judgement value for the comparison function. Setting range: 1 to 16 (The values out of the setting range are invalid.)	Times
UM 00080 UM 00150 UM 00220 UM 002F0	Comparison data 0	H0	- Areas in which the output patterns of comparison data and comparison match flags are stored. - The formats of storage areas differ between the target value match comparison and the band comparison. - Each item occupies 8-word area. The unit memory numbers (UM) indicate starting addresses. - For details of the format of target value match comparison, refer to 7.1.2 Target Value Match Comparison and Band Comparison. - For details of the format of band comparison, refer to 7.3.3 Configuration of Band Comparison.	—
UM 00088 UM 00158 UM 00228 UM 002F8	Comparison data 1	H0		—
UM 00090 UM 00160 UM 00230 UM 00300	Comparison data 2	H0		—
UM 00098 UM 00168 UM 00238 UM 00308	Comparison data 3	H0		—
UM 000A0 UM 00170 UM 00240 UM 00310	Comparison data 4	H0		—
UM 000A8 UM 00178 UM 00248 UM 00318	Comparison data 5	H0		—
UM 000B0 UM 00180 UM 00250 UM 00320	Comparison data 6	H0		—

(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

■ Comparison function

Unit memory No.(Hex)	Name	Default	Setting range and description	Unit
UM 000B8 UM 00188 UM 00258 UM 00328	Comparison data 7	H0	- Set the data for band comparison or target value match comparison. - The formats to be set differ between the band comparison and the target value match comparison. - Each item occupies 8-word area. The unit memory numbers (UM) indicate starting addresses. - For details of the format of target value match comparison, refer to 7.1.2 Target Value Match Comparison and Band Comparison. - For details of the format of band comparison, refer to 7.3.3 Configuration of Band Comparison.	—
UM 000C0 UM 00190 UM 00260 UM 00330	Comparison data 8	H0		—
UM 000C8 UM 00198 UM 00268 UM 00338	Comparison data 9	H0		—
UM 000D0 UM 001A0 UM 00270 UM 00340	Comparison data 10	H0		—
UM 000D8 UM 001A8 UM 00278 UM 00348	Comparison data 11	H0		—
UM 000E0 UM 001B0 UM 00280 UM 00350	Comparison data 12	H0		—
UM 000E8 UM 001B8 UM 00288 UM 00358	Comparison data 13	H0		—
UM 000F0 UM 001C0 UM 00290 UM 00360	Comparison data 14	H0		—
UM 000F8 UM 001C8 UM 00298 UM 00368	Comparison data 15	H0		—

(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

■ **External output function**

Unit memory No.(Hex)	Name	Default	Setting range and description	Unit
UM 00100 UM 001D0 UM 002A0 UM 00370	External output 0 signal setting	H0	Set whether or not to output the comparison match 0 flag to the external output 0 signal. H0: Not output H1: Output	—
UM 00101 UM 001D1 UM 002A1 UM 00371	External output 0 signal output hold setting	H0	Set whether or not to hold the output signal in the program mode when an error occurs. H0: Not hold H1: Hold	—
UM 00102 UM 001D2 UM 002A2 UM 00372	External output 0 signal ON timing delay	U0	Set the ON timing delay of external output 0 signal. Setting range: 0 to 1,000 (The values out of the setting range are invalid.)	ms
UM 00103 UM 001D3 UM 002A3 UM 00373	External output 0 signal ON hold time	U0	Set the ON hold time of external output 0 signal. Setting range: 0 to 1,000 (The values out of the setting range are invalid.)	ms
UM 00104 UM 001D4 UM 002A4 UM 00374	External output 1 signal setting	H0	Set whether or not to output the comparison match 1 flag to the external output 1 signal. H0: Not output H1: Output	—
UM 00105 UM 001D5 UM 002A5 UM 00375	External output 1 signal output hold setting	H0	Set whether or not to hold the output signal in the program mode when an error occurs. H0: Not hold H1: Hold	—
UM 00106 UM 001D6 UM 002A6 UM 00376	External output 1 signal ON timing delay	U0	Set the ON timing delay of external output 1 signal. Setting range: 0 to 1,000 (The values out of the setting range are invalid.)	ms
UM 00107 UM 001D7 UM 002A7 UM 00377	External output 1 signal ON hold time	U0	Set the ON hold time of external output 1 signal. Setting range: 0 to 1,000(The values out of the setting range are invalid.)	ms

(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

■ Capture function

Unit memory No.（Hex）	Name	Default	Setting range and description	Unit
UM 00110 UM 001E0 UM 002B0 UM 00380	Capture 0 setting	H0	Make the setting for the capture function or sampling capture function. H0: Not use capture 0 function H1: Capture function at rising edge of control 0 signal H2: Capture function at trailing edge of control 0 signal H3: Capture function at rising edge of control 1 signal H4: Capture function at trailing edge of control 1 signal H5: Control 0 signal positive logic sampling capture function H6: Control 0 signal negative logic sampling capture function H7: Control 1 signal positive logic sampling capture function H8: Control 1 signal negative logic sampling capture function H9: Output relay (Y relay) sampling capture function The capture 1 setting area is invalid when the sampling capture function (H5 to H9) is selected in the capture 0 setting.	—
UM 00111 UM 001E1 UM 002B1 UM 00381	Capture 1 setting	H0	Make the setting for the capture function or sampling capture function. H0: Not use capture 1 function H1: Capture function at rising edge of control 0 signal H2: Capture function at trailing edge of control 0 signal H3: Capture function at rising edge of control 1 signal H4: Capture function at trailing edge of control 1 signal However, this setting area is invalid when the sampling capture function (H5 to H9) is selected in the capture 0 setting.	—
UM 00112 UM 001E2 UM 002B2 UM 00382	Capture function operation setting	H1	Make the setting for the capture function or sampling capture function. H0: One operation H1: Continuous operation	—
UM 00113 UM 001E3 UM 002B3 UM 00383	Sampling time	U1	Set a sampling time. Setting range: 1 to 65,535 (The values out of the setting range are invalid.)	ms

(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

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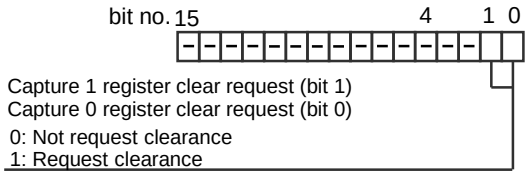
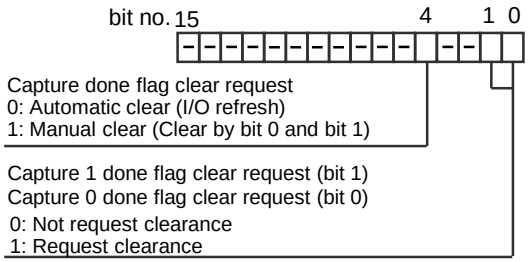
■ **Capture function / Interrupt function**

<table>
<tr><th>Unit memory No.（Hex）</th><th>Name</th><th>Default</th><th>Setting range and description</th><th>Unit</th></tr>
<tr><td>UM 00114
UM 001E4
UM 002B4
UM 00384</td><td>Capture value clear request</td><td>H0</td><td>● Clears values stored in the capture registers and capture register buffers.
● To clear the capture 0 register, turn off, on and off the bit 0 of the unit memory. To clear the capture 1 register, turn off, on and off the bit 1 of the unit memory.
● Clears the areas of capture 0 register, capture 0 register buffer and register difference value buffer when requesting the capture 0 by executing the clearance of the capture 0 register.
● Clears the areas of capture 1 register, capture 1 register buffer and register difference value buffer when requesting the capture 1 by executing the clearance of the capture 1 register.
  </td><td>—</td></tr>
<tr><td>UM 00115
UM 001E5
UM 002B5
UM 00385</td><td>Capture done flag clear request (Edge type)</td><td>H0</td><td>It is used to reset the capture 0 done flag and capture 1 done flag using user programs. To reset the capture 0 done flag, write H11 and then H10. To reset the capture 0 done flag, write H12 and then H10.At the default setting, the request to clear the capture done flag is automatically made at the time of I/O refresh.
  </td><td>—</td></tr>
<tr><td>UM 00118
UM 001E8
UM 002B8
UM 00388</td><td>Interrupt function enable/disable setting</td><td>H3</td><td>Make the settings for the interrupt operation at the time of comparison match.<table><tr><th>bit</th><th>Default</th><th>Description</th><th>Setting</th></tr><tr><td>0</td><td>1</td><td>Comparison match 0 flag</td><td rowspan="2">0: Disable
1: Enable</td></tr><tr><td>1</td><td>1</td><td>Comparison match 1 flag</td></tr><tr><td>15-2</td><td>-</td><td>-</td><td>-</td></tr></table></td><td>—</td></tr>
</table>

(Note 1) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

(Note 2) The capture value clear request and capture done flag clear request signals are available from the high-speed counter unit Ver.1.2. They can be set in user programs.

(Note 3) Even if the capture value clear request is executed, the number of completed capture operations in the buffer area will not be cleared. The number of completed capture operations will be cleared when the capture enable request (Y7) or the sampling capture function is activated.

11.4.3 Monitor Display Area

Unit memory No. (Hex)	Name	Default	Setting range and description	Unit
UM 003A0 - UM 003A1 UM 003B0 - UM 003B1 UM 003C0 - UM 003C1 UM 003D0 - UM 003D1	Count value	K0	Current count value of counter Range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
UM 003A2 - UM 003A3 UM 003B2 - UM 003B3 UM 003C2 - UM 003C3 UM 003D2 - UM 003D3	Capture 0 register	K0	Value of capture 0 register. Range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
UM 003A4 - UM 003A5 UM 003B4 - UM 003B5 UM 003C4 - UM 003C5 UM 003D4 - UM 003D5	Capture 1 register	K0	Value of capture 1 register. Range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
UM 003A6 - UM 003A7 UM 003B6 - UM 003B7 UM 003C6 - UM 003C7 UM 003D6 - UM 003D7	Capture register difference value	K0	Calculated difference between the capature registers (Capture 1 register - Capture 0 register) Range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
UM 003A8 - UM 003A9 UM 003B8 - UM 003B9 UM 003C8 - UM 003C9 UM 003D8 - UM 003D9	Frequency measurement (Averaging)	U0	Frequency measurement value after averaging procedure. Range: 0 to 20,000,000 Signed 32-bit	Hz
UM 003AA -UM 003AB UM 003BA -UM 003BB UM 003CA - UM 003CB UM 003DA - UM 003DB	Rotation speed measurement (Averaging)	U0	Rotation speed measurement value after averaging procedure Range: -1,200,000,000 to +1,200,000,000 Signed 32-bit	rpm

(Note) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

11.4.4 Capture Value Buffer Area

■ **Capture value buffer area (For capture 0)**

Unit memory No. (Hex)	Name	Default	Setting range and description	Unit
UM 00400 UM 00600 UM 00800 UM 00A00	Number of completed capture 0 operations	U0	Monitors the number of completed capture 0 operations while capturing is enabled. It is cleared to zero when the capture enable request (Y7, Y17, Y27 or Y37) is activated.	Times
UM 00402 - UM 00403 UM 00602 - UM 00603 UM 00802 - UM 00803 UM 00A02 - UM 00A03	Capture 0 register buffer 1	K0	Once the capture processing is performed, the data stored in the capture 0 registers (UM 003x2 – UM 003x3) are transferred to the buffer 1. The data are shifted and stored from the buffer 1 to buffer 60 sequentially. Range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
(Omitted)	(Omitted)			
UM 00478 - UM 00479 UM 00678 - UM 00679 UM 00878 - UM 00879 UM 00A78 - UM 00A79	Capture 0 register Buffer 60			
UM 00482 - UM 00483 UM 00682 - UM 00683 UM 00882 - UM 00883 UM 00A82 - UM 00A83	Capture register difference value for capture 0 request Buffer 1	K0	Transfers the difference between the capture 1 register (UM 003x4 - UM 003x5) and the capture 0 register (UM 003x2 - UM 003x3) to the buffer 1 when the capture request is made for the capture 0. The data are shifted and stored from the buffer 1 to buffer 60 sequentially. Range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
(Omitted)	(Omitted)			
UM 004F8 - UM 004F9 UM 006F8 - UM 006F9 UM 008F8 - UM 008F9 UM 00AF8 - UM 00AF9	Capture register difference value for capture 0 request Buffer 60			

(Note 1) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.
(Note 2) The capture value buffer areas are available from the high-speed counter unit Ver.1.2.

◆ **REFERENCE**

- **For information on unit memory (UM) numbers corresponding to each buffer number, refer to the list beginning on page 11-23.**

■ **Capture value buffer area (For capture 1)**

Unit memory No. (Hex)	Name	Default	Setting range and description	Unit
UM 00500 UM 00700 UM 00900 UM 00B00	Number of completed capture 1 operations	U0	Monitors the number of completed capture 1 operations while capturing is enabled. It is cleared to zero when the capture enable request (Y7, Y17, Y27 or Y37) is activated.	Times
UM 00502 - UM 00503 UM 00702 - UM 00703 UM 00902 - UM 00903 UM 00B02 - UM 00B03	Capture 1 Register Buffer 1	K0	Once the capture processing is performed, the data stored in the capture 1 registers (UM 003x4 - UM 003x5) are transferred to the buffer 1. The data are shifted and stored from the buffer 1 to buffer 60 sequentially. Range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
(Omitted)	(Omitted)			
UM 00578 - UM 00579 UM 00778 - UM 00779 UM 00978 - UM 00979 UM 00B78 - UM 00B79	Capture 1 register Buffer 60			
UM 00582 - UM 00583 UM 00782 - UM 00783 UM 00982 - UM 00983 UM 00B82 - UM 00B83	Capture register difference value for capture 1 request Buffer 1	K0	Transfers the difference between the capture 1 register (UM 003x4 - UM 003x5) and the capture 0 register (UM 003x2 - UM 003x3) to the buffer 1 when the capture request is made for the capture 1. The data are shifted and stored from the buffer 1 to buffer 60 sequentially. Range: -2,147,483,648 (8000 0000H) to 2,147,483,647 (7FFF FFFFH) Signed 32-bit	Pulse
(Omitted)	(Omitted)			
UM 005F8 - UM 005F9 UM 007F8 - UM 007F9 UM 009F8 - UM 009F9 UM 00BF8 - UM 00BF9	Capture register difference value for capture 1 request Buffer 60			

(Note 1) The unit memory numbers in the above table are for CH0, CH1, CH2 and CH3 from the top.

(Note 2) The capture value buffer areas are available from the high-speed counter unit Ver.1.2.

◆ **REFERENCE**

- **For information on unit memory (UM) numbers corresponding to each buffer number, refer to the list beginning on page 11-27.**

■ **Check list of unit memories (Capture 0 register buffers)**

Buffer No.	Unit memory (UM) No.			
	CH0	CH1	CH2	CH3
Buffer 1	UM00402-UM00403	UM00602-UM00603	UM00802-UM00803	UM00A02-UM00A03
Buffer 2	UM00404-UM00405	UM00604-UM00605	UM00804-UM00805	UM00A04-UM00A05
Buffer 3	UM00406-UM00407	UM00606-UM00607	UM00806-UM00807	UM00A06-UM00A07
Buffer 4	UM00408-UM00409	UM00608-UM00609	UM00808-UM00809	UM00A08-UM00A09
Buffer 5	UM0040A-UM0040B	UM0060A-UM0060B	UM0080A-UM0080B	UM00A0A-UM00A0B
Buffer 6	UM0040C-UM0040D	UM0060C-UM0060D	UM0080C-UM0080D	UM00A0C-UM00A0D
Buffer 7	UM0040E-UM0040F	UM0060E-UM0060F	UM0080E-UM0080F	UM00A0E-UM00A0F
Buffer 8	UM00410-UM00411	UM00610-UM00611	UM00810-UM00811	UM00A10-UM00A11
Buffer 9	UM00412-UM00413	UM00612-UM00613	UM00812-UM00813	UM00A12-UM00A13
Buffer 10	UM00414-UM00415	UM00614-UM00615	UM00814-UM00815	UM00A14-UM00A15
Buffer 11	UM00416-UM00417	UM00616-UM00617	UM00816-UM00817	UM00A16-UM00A17
Buffer 12	UM00418-UM00419	UM00618-UM00619	UM00818-UM00819	UM00A18-UM00A19
Buffer 13	UM0041A-UM0041B	UM0061A-UM0061B	UM0081A-UM0081B	UM00A1A-UM00A1B
Buffer 14	UM0041C-UM0041D	UM0061C-UM0061D	UM0081C-UM0081D	UM00A1C-UM00A1D
Buffer 15	UM0041E-UM0041F	UM0061E-UM0061F	UM0081E-UM0081F	UM00A1E-UM00A1F
Buffer 16	UM00420-UM00421	UM00620-UM00621	UM00820-UM00821	UM00A20-UM00A21
Buffer 17	UM00422-UM00423	UM00622-UM00623	UM00822-UM00823	UM00A22-UM00A23
Buffer 18	UM00424-UM00425	UM00624-UM00625	UM00824-UM00825	UM00A24-UM00A25
Buffer 19	UM00426-UM00427	UM00626-UM00627	UM00826-UM00827	UM00A26-UM00A27
Buffer 20	UM00428-UM00429	UM00628-UM00629	UM00828-UM00829	UM00A28-UM00A29
Buffer 21	UM0042A-UM0042B	UM0062A-UM0062B	UM0082A-UM0082B	UM00A2A-UM00A2B
Buffer 22	UM0042C-UM0042D	UM0062C-UM0062D	UM0082C-UM0082D	UM00A2C-UM00A2D
Buffer 23	UM0042E-UM0042F	UM0062E-UM0062F	UM0082E-UM0082F	UM00A2E-UM00A2F
Buffer 24	UM00430-UM00431	UM00630-UM00631	UM00830-UM00831	UM00A30-UM00A31
Buffer 25	UM00432-UM00433	UM00632-UM00633	UM00832-UM00833	UM00A32-UM00A33
Buffer 26	UM00434-UM00435	UM00634-UM00635	UM00834-UM00835	UM00A34-UM00A35
Buffer 27	UM00436-UM00437	UM00636-UM00637	UM00836-UM00837	UM00A36-UM00A37
Buffer 28	UM00438-UM00439	UM00638-UM00639	UM00838-UM00839	UM00A38-UM00A39
Buffer 29	UM0043A-UM0043B	UM0063A-UM0063B	UM0083A-UM0083B	UM00A3A-UM00A3B
Buffer 30	UM0043C-UM0043D	UM0063C-UM0063D	UM0083C-UM0083D	UM00A3C-UM00A3D

(Note 1) The capture value buffer areas are available from the high-speed counter unit Ver.1.2.

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■ **Check list of unit memories (Capture 0 register buffers)**

Buffer No.	Unit memory (UM) No.			
	CH0	CH1	CH2	CH3
Buffer 31	UM0043E-UM0043F	UM0063E-UM0063F	UM0083E-UM0083F	UM00A3E-UM00A3F
Buffer 32	UM00440-UM00441	UM00640-UM00641	UM00840-UM00841	UM00A40-UM00A41
Buffer 33	UM00442-UM00443	UM00642-UM00643	UM00842-UM00843	UM00A42-UM00A43
Buffer 34	UM00444-UM00445	UM00644-UM00645	UM00844-UM00845	UM00A44-UM00A45
Buffer 35	UM00446-UM00447	UM00646-UM00647	UM00846-UM00847	UM00A46-UM00A47
Buffer 36	UM00448-UM00449	UM00648-UM00649	UM00848-UM00849	UM00A48-UM00A49
Buffer 37	UM0044A-UM0044B	UM0064A-UM0064B	UM0084A-UM0084B	UM00A4A-UM00A4B
Buffer 38	UM0044C-UM0044D	UM0064C-UM0064D	UM0084C-UM0084D	UM00A4C-UM00A4D
Buffer 39	UM0044E-UM0044F	UM0064E-UM0064F	UM0084E-UM0084F	UM00A4E-UM00A4F
Buffer 40	UM00450-UM00451	UM00650-UM00651	UM00850-UM00851	UM00A50-UM00A51
Buffer 41	UM00452-UM00453	UM00652-UM00653	UM00852-UM00853	UM00A52-UM00A53
Buffer 42	UM00454-UM00455	UM00654-UM00655	UM00854-UM00855	UM00A54-UM00A55
Buffer 43	UM00456-UM00457	UM00656-UM00657	UM00856-UM00857	UM00A56-UM00A57
Buffer 44	UM00458-UM00459	UM00658-UM00659	UM00858-UM00859	UM00A58-UM00A59
Buffer 45	UM0045A-UM0045B	UM0065A-UM0065B	UM0085A-UM0085B	UM00A5A-UM00A5B
Buffer 46	UM0045C-UM0045D	UM0065C-UM0065D	UM0085C-UM0085D	UM00A5C-UM00A5D
Buffer 47	UM0045E-UM0045F	UM0065E-UM0065F	UM0085E-UM0085F	UM00A5E-UM00A5F
Buffer 48	UM00460-UM00461	UM00660-UM00661	UM00860-UM00861	UM00A60-UM00A61
Buffer 49	UM00462-UM00463	UM00662-UM00663	UM00862-UM00863	UM00A62-UM00A63
Buffer 50	UM00464-UM00465	UM00664-UM00665	UM00864-UM00865	UM00A64-UM00A65
Buffer 51	UM00466-UM00467	UM00666-UM00667	UM00866-UM00867	UM00A66-UM00A67
Buffer 52	UM00468-UM00469	UM00668-UM00669	UM00868-UM00869	UM00A68-UM00A69
Buffer 53	UM0046A-UM0046B	UM0066A-UM0066B	UM0086A-UM0086B	UM00A6A-UM00A6B
Buffer 54	UM0046C-UM0046D	UM0066C-UM0066D	UM0086C-UM0086D	UM00A6C-UM00A6D
Buffer 55	UM0046E-UM0046F	UM0066E-UM0066F	UM0086E-UM0086F	UM00A6E-UM00A6F
Buffer 56	UM00470-UM00471	UM00670-UM00671	UM00870-UM00871	UM00A70-UM00A71
Buffer 57	UM00472-UM00473	UM00672-UM00673	UM00872-UM00873	UM00A72-UM00A73
Buffer 58	UM00474-UM00475	UM00674-UM00675	UM00874-UM00875	UM00A74-UM00A75
Buffer 59	UM00476-UM00477	UM00676-UM00677	UM00876-UM00877	UM00A76-UM00A77
Buffer 60	UM00478-UM00479	UM00678-UM00679	UM00878-UM00879	UM00A78-UM00A79

(Note 1) The capture value buffer areas are available from the high-speed counter unit Ver.1.2.

■ **Check list of unit memories (Difference value buffer: Stored when Capture 0 request occurs.)**

Buffer No.	Unit memory (UM) No.			
	CH0	CH1	CH2	CH3
Buffer 1	UM00482-UM00483	UM00682-UM00683	UM00882-UM00883	UM00A82-UM00A83
Buffer 2	UM00484-UM00485	UM00684-UM00685	UM00884-UM00885	UM00A84-UM00A85
Buffer 3	UM00486-UM00487	UM00686-UM00687	UM00886-UM00887	UM00A86-UM00A87
Buffer 4	UM00488-UM00489	UM00688-UM00689	UM00888-UM00889	UM00A88-UM00A89
Buffer 5	UM0048A-UM0048B	UM0068A-UM0068B	UM0088A-UM0088B	UM00A8A-UM00A8B
Buffer 6	UM0048C-UM0048D	UM0068C-UM0068D	UM0088C-UM0088D	UM00A8C-UM00A8D
Buffer 7	UM0048E-UM0048F	UM0068E-UM0068F	UM0088E-UM0088F	UM00A8E-UM00A8F
Buffer 8	UM00490-UM00491	UM00690-UM00691	UM00890-UM00891	UM00A90-UM00A91
Buffer 9	UM00492-UM00493	UM00692-UM00693	UM00892-UM00893	UM00A92-UM00A93
Buffer 10	UM00494-UM00495	UM00694-UM00695	UM00894-UM00895	UM00A94-UM00A95
Buffer 11	UM00496-UM00497	UM00696-UM00697	UM00896-UM00897	UM00A96-UM00A97
Buffer 12	UM00498-UM00499	UM00698-UM00699	UM00898-UM00899	UM00A98-UM00A99
Buffer 13	UM0049A-UM0049B	UM0069A-UM0069B	UM0089A-UM0089B	UM00A9A-UM00A9B
Buffer 14	UM0049C-UM0049D	UM0069C-UM0069D	UM0089C-UM0089D	UM00A9C-UM00A9D
Buffer 15	UM0049E-UM0049F	UM0069E-UM0069F	UM0089E-UM0089F	UM00A9E-UM00A9F
Buffer 16	UM004A0-UM004A1	UM006A0-UM006A1	UM008A0-UM008A1	UM00AA0-UM00AA1
Buffer 17	UM004A2-UM004A3	UM006A2-UM006A3	UM008A2-UM008A3	UM00AA2-UM00AA3
Buffer 18	UM004A4-UM004A5	UM006A4-UM006A5	UM008A4-UM008A5	UM00AA4-UM00AA5
Buffer 19	UM004A6-UM004A7	UM006A6-UM006A7	UM008A6-UM008A7	UM00AA6-UM00AA7
Buffer 20	UM004A8-UM004A9	UM006A8-UM006A9	UM008A8-UM008A9	UM00AA8-UM00AA9
Buffer 21	UM004AA-UM004AB	UM006AA-UM006AB	UM008AA-UM008AB	UM00AAA-UM00AAB
Buffer 22	UM004AC-UM004AD	UM006AC-UM006AD	UM008AC-UM008AD	UM00AAC-UM00AAD
Buffer 23	UM004AE-UM004AF	UM006AE-UM006AF	UM008AE-UM008AF	UM00AAE-UM00AAF
Buffer 24	UM004B0-UM004B1	UM006B0-UM006B1	UM008B0-UM008B1	UM00AB0-UM00AB1
Buffer 25	UM004B2-UM004B3	UM006B2-UM006B3	UM008B2-UM008B3	UM00AB2-UM00AB3
Buffer 26	UM004B4-UM004B5	UM006B4-UM006B5	UM008B4-UM008B5	UM00AB4-UM00AB5
Buffer 27	UM004B6-UM004B7	UM006B6-UM006B7	UM008B6-UM008B7	UM00AB6-UM00AB7
Buffer 28	UM004B8-UM004B9	UM006B8-UM006B9	UM008B8-UM008B9	UM00AB8-UM00AB9
Buffer 29	UM004BA-UM004BB	UM006BA-UM006BB	UM008BA-UM008BB	UM00ABA-UM00ABB
Buffer 30	UM004BC-UM004BD	UM006BC-UM006BD	UM008BC-UM008BD	UM00ABC-UM00ABD

(Note 1) The capture value buffer areas are available from the high-speed counter unit Ver.1.2.

(Note 2) In the above areas, the capture register difference values (Capture 1 register 1 - Capture 0 register) are stored when capturing for the capture 0 register is executed.

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■ **Check list of unit memories (Difference value buffer: Stored when Capture 0 request occurs.)**

Buffer No.	Unit memory (UM) No.			
	CH0	CH1	CH2	CH3
Buffer 31	UM004BE-UM004BF	UM006BE-UM006BF	UM008BE-UM008BF	UM00ABE-UM00ABF
Buffer 32	UM004C0-UM004C1	UM006C0-UM006C1	UM008C0-UM008C1	UM00AC0-UM00AC1
Buffer 33	UM004C2-UM004C3	UM006C2-UM006C3	UM008C2-UM008C3	UM00AC2-UM00AC3
Buffer 34	UM004C4-UM004C5	UM006C4-UM006C5	UM008C4-UM008C5	UM00AC4-UM00AC5
Buffer 35	UM004C6-UM004C7	UM006C6-UM006C7	UM008C6-UM008C7	UM00AC6-UM00AC7
Buffer 36	UM004C8-UM004C9	UM006C8-UM006C9	UM008C8-UM008C9	UM00AC8-UM00AC9
Buffer 37	UM004CA-UM004CB	UM006CA-UM006CB	UM008CA-UM008CB	UM00ACA-UM00ACB
Buffer 38	UM004CC-UM004CD	UM006CC-UM006CD	UM008CC-UM008CD	UM00ACC-UM00ACD
Buffer 39	UM004CE-UM004CF	UM006CE-UM006CF	UM008CE-UM008CF	UM00ACE-UM00ACF
Buffer 40	UM004D0-UM004D1	UM006D0-UM006D1	UM008D0-UM008D1	UM00AD0-UM00AD1
Buffer 41	UM004D2-UM004D3	UM006D2-UM006D3	UM008D2-UM008D3	UM00AD2-UM00AD3
Buffer 42	UM004D4-UM004D5	UM006D4-UM006D5	UM008D4-UM008D5	UM00AD4-UM00AD5
Buffer 43	UM004D6-UM004D7	UM006D6-UM006D7	UM008D6-UM008D7	UM00AD6-UM00AD7
Buffer 44	UM004D8-UM004D9	UM006D8-UM006D9	UM008D8-UM008D9	UM00AD8-UM00AD9
Buffer 45	UM004DA-UM004DB	UM006DA-UM006DB	UM008DA-UM008DB	UM00ADA-UM00ADB
Buffer 46	UM004DC-UM004DD	UM006DC-UM006DD	UM008DC-UM008DD	UM00ADC-UM00ADD
Buffer 47	UM004DE-UM004DF	UM006DE-UM006DF	UM008DE-UM008DF	UM00ADE-UM00ADF
Buffer 48	UM004E0-UM004E1	UM006E0-UM006E1	UM008E0-UM008E1	UM00AE0-UM00AE1
Buffer 49	UM004E2-UM004E3	UM006E2-UM006E3	UM008E2-UM008E3	UM00AE2-UM00AE3
Buffer 50	UM004E4-UM004E5	UM006E4-UM006E5	UM008E4-UM008E5	UM00AE4-UM00AE5
Buffer 51	UM004E6-UM004E7	UM006E6-UM006E7	UM008E6-UM008E7	UM00AE6-UM00AE7
Buffer 52	UM004E8-UM004E9	UM006E8-UM006E9	UM008E8-UM008E9	UM00AE8-UM00AE9
Buffer 53	UM004EA-UM004EB	UM006EA-UM006EB	UM008EA-UM008EB	UM00AEA-UM00AEB
Buffer 54	UM004EC-UM004ED	UM006EC-UM006ED	UM008EC-UM008ED	UM00AEC-UM00AED
Buffer 55	UM004EE-UM004EF	UM006EE-UM006EF	UM008EE-UM008EF	UM00AEE-UM00AEF
Buffer 56	UM004F0-UM004F1	UM006F0-UM006F1	UM008F0-UM008F1	UM00AF0-UM00AF1
Buffer 57	UM004F2-UM004F3	UM006F2-UM006F3	UM008F2-UM008F3	UM00AF2-UM00AF3
Buffer 58	UM004F4-UM004F5	UM006F4-UM006F5	UM008F4-UM008F5	UM00AF4-UM00AF5
Buffer 59	UM004F6-UM004F7	UM006F6-UM006F7	UM008F6-UM008F7	UM00AF6-UM00AF7
Buffer 60	UM004F8-UM004F9	UM006F8-UM006F9	UM008F8-UM008F9	UM00AF8-UM00AF9

(Note 1) The capture value buffer areas are available from the high-speed counter unit Ver.1.2.

(Note 2) In the above areas, the capture register difference values (Capture 1 register 1 - Capture 0 register) are stored when capturing for the capture 0 register is executed.

■ **Check list of unit memories (Capture 1 register buffers)**

Buffer No.	Unit memory (UM) No.			
	CH0	CH1	CH2	CH3
Buffer 1	UM00502-UM00503	UM00702-UM00703	UM00902-UM00903	UM00B02-UM00B03
Buffer 2	UM00504-UM00505	UM00704-UM00705	UM00904-UM00905	UM00B04-UM00B05
Buffer 3	UM00506-UM00507	UM00706-UM00707	UM00906-UM00907	UM00B06-UM00B07
Buffer 4	UM00508-UM00509	UM00708-UM00709	UM00908-UM00909	UM00B08-UM00B09
Buffer 5	UM0050A-UM0050B	UM0070A-UM0070B	UM0090A-UM0090B	UM00B0A-UM00B0B
Buffer 6	UM0050C-UM0050D	UM0070C-UM0070D	UM0090C-UM0090D	UM00B0C-UM00B0D
Buffer 7	UM0050E-UM0050F	UM0070E-UM0070F	UM0090E-UM0090F	UM00B0E-UM00B0F
Buffer 8	UM00510-UM00511	UM00710-UM00711	UM00910-UM00911	UM00B10-UM00B11
Buffer 9	UM00512-UM00513	UM00712-UM00713	UM00912-UM00913	UM00B12-UM00B13
Buffer 10	UM00514-UM00515	UM00714-UM00715	UM00914-UM00915	UM00B14-UM00B15
Buffer 11	UM00516-UM00517	UM00716-UM00717	UM00916-UM00917	UM00B16-UM00B17
Buffer 12	UM00518-UM00519	UM00718-UM00719	UM00918-UM00919	UM00B18-UM00B19
Buffer 13	UM0051A-UM0051B	UM0071A-UM0071B	UM0091A-UM0091B	UM00B1A-UM00B1B
Buffer 14	UM0051C-UM0051D	UM0071C-UM0071D	UM0091C-UM0091D	UM00B1C-UM00B1D
Buffer 15	UM0051E-UM0051F	UM0071E-UM0071F	UM0091E-UM0091F	UM00B1E-UM00B1F
Buffer 16	UM00520-UM00521	UM00720-UM00721	UM00920-UM00921	UM00B20-UM00B21
Buffer 17	UM00522-UM00523	UM00722-UM00723	UM00922-UM00923	UM00B22-UM00B23
Buffer 18	UM00524-UM00525	UM00724-UM00725	UM00924-UM00925	UM00B24-UM00B25
Buffer 19	UM00526-UM00527	UM00726-UM00727	UM00926-UM00927	UM00B26-UM00B27
Buffer 20	UM00528-UM00529	UM00728-UM00729	UM00928-UM00929	UM00B28-UM00B29
Buffer 21	UM0052A-UM0052B	UM0072A-UM0072B	UM0092A-UM0092B	UM00B2A-UM00B2B
Buffer 22	UM0052C-UM0052D	UM0072C-UM0072D	UM0092C-UM0092D	UM00B2C-UM00B2D
Buffer 23	UM0052E-UM0052F	UM0072E-UM0072F	UM0092E-UM0092F	UM00B2E-UM00B2F
Buffer 24	UM00530-UM00531	UM00730-UM00731	UM00930-UM00931	UM00B30-UM00B31
Buffer 25	UM00532-UM00533	UM00732-UM00733	UM00932-UM00933	UM00B32-UM00B33
Buffer 26	UM00534-UM00535	UM00734-UM00735	UM00934-UM00935	UM00B34-UM00B35
Buffer 27	UM00536-UM00537	UM00736-UM00737	UM00936-UM00937	UM00B36-UM00B37
Buffer 28	UM00538-UM00539	UM00738-UM00739	UM00938-UM00939	UM00B38-UM00B39
Buffer 29	UM0053A-UM0053B	UM0073A-UM0073B	UM0093A-UM0093B	UM00B3A-UM00B3B
Buffer 30	UM0053C-UM0053D	UM0073C-UM0073D	UM0093C-UM0093D	UM00B3C-UM00B3D

(Note 1) The capture value buffer areas are available from the high-speed counter unit Ver.1.2.

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■ **Check list of unit memories (Capture 1 register buffers)**

Buffer No.	Unit memory (UM) No.			
	CH0	CH1	CH2	CH3
Buffer 31	UM0053E-UM0053F	UM0073E-UM0073F	UM0093E-UM0093F	UM00B3E-UM00B3F
Buffer 32	UM00540-UM00541	UM00740-UM00741	UM00940-UM00941	UM00B40-UM00B41
Buffer 33	UM00542-UM00543	UM00742-UM00743	UM00942-UM00943	UM00B42-UM00B43
Buffer 34	UM00544-UM00545	UM00744-UM00745	UM00944-UM00945	UM00B44-UM00B45
Buffer 35	UM00546-UM00547	UM00746-UM00747	UM00946-UM00947	UM00B46-UM00B47
Buffer 36	UM00548-UM00549	UM00748-UM00749	UM00948-UM00949	UM00B48-UM00B49
Buffer 37	UM0054A-UM0054B	UM0074A-UM0074B	UM0094A-UM0094B	UM00B4A-UM00B4B
Buffer 38	UM0054C-UM0054D	UM0074C-UM0074D	UM0094C-UM0094D	UM00B4C-UM00B4D
Buffer 39	UM0054E-UM0054F	UM0074E-UM0074F	UM0094E-UM0094F	UM00B4E-UM00B4F
Buffer 40	UM00550-UM00551	UM00750-UM00751	UM00950-UM00951	UM00B50-UM00B51
Buffer 41	UM00552-UM00553	UM00752-UM00753	UM00952-UM00953	UM00B52-UM00B53
Buffer 42	UM00554-UM00555	UM00754-UM00755	UM00954-UM00955	UM00B54-UM00B55
Buffer 43	UM00556-UM00557	UM00756-UM00757	UM00956-UM00957	UM00B56-UM00B57
Buffer 44	UM00558-UM00559	UM00758-UM00759	UM00958-UM00959	UM00B58-UM00B59
Buffer 45	UM0055A-UM0055B	UM0075A-UM0075B	UM0095A-UM0095B	UM00B5A-UM00B5B
Buffer 46	UM0055C-UM0055D	UM0075C-UM0075D	UM0095C-UM0095D	UM00B5C-UM00B5D
Buffer 47	UM0055E-UM0055F	UM0075E-UM0075F	UM0095E-UM0095F	UM00B5E-UM00B5F
Buffer 48	UM00560-UM00561	UM00760-UM00761	UM00960-UM00961	UM00B60-UM00B61
Buffer 49	UM00562-UM00563	UM00762-UM00763	UM00962-UM00963	UM00B62-UM00B63
Buffer 50	UM00564-UM00565	UM00764-UM00765	UM00964-UM00965	UM00B64-UM00B65
Buffer 51	UM00566-UM00567	UM00766-UM00767	UM00966-UM00967	UM00B66-UM00B67
Buffer 52	UM00568-UM00569	UM00768-UM00769	UM00968-UM00969	UM00B68-UM00B69
Buffer 53	UM0056A-UM0056B	UM0076A-UM0076B	UM0096A-UM0096B	UM00B6A-UM00B6B
Buffer 54	UM0056C-UM0056D	UM0076C-UM0076D	UM0096C-UM0096D	UM00B6C-UM00B6D
Buffer 55	UM0056E-UM0056F	UM0076E-UM0076F	UM0096E-UM0096F	UM00B6E-UM00B6F
Buffer 56	UM00570-UM00571	UM00770-UM00771	UM00970-UM00971	UM00B70-UM00B71
Buffer 57	UM00572-UM00573	UM00772-UM00773	UM00972-UM00973	UM00B72-UM00B73
Buffer 58	UM00574-UM00575	UM00774-UM00775	UM00974-UM00975	UM00B74-UM00B75
Buffer 59	UM00576-UM00577	UM00776-UM00777	UM00976-UM00977	UM00B76-UM00B77
Buffer 60	UM00578-UM00579	UM00778-UM00779	UM00978-UM00979	UM00B78-UM00B79

(Note 1) The capture value buffer areas are available from the high-speed counter unit Ver.1.2.

■ **Check list of unit memories (Difference value buffer: Stored when Capture 1 request occurs.)**

Buffer No.	Unit memory (UM) No.			
	CH0	CH1	CH2	CH3
Buffer 1	UM00582-UM00583	UM00782-UM00783	UM00982-UM00983	UM00B82-UM00B83
Buffer 2	UM00584-UM00585	UM00784-UM00785	UM00984-UM00985	UM00B84-UM00B85
Buffer 3	UM00586-UM00587	UM00786-UM00787	UM00986-UM00987	UM00B86-UM00B87
Buffer 4	UM00588-UM00589	UM00788-UM00789	UM00988-UM00989	UM00B88-UM00B89
Buffer 5	UM0058A-UM0058B	UM0078A-UM0078B	UM0098A-UM0098B	UM00B8A-UM00B8B
Buffer 6	UM0058C-UM0058D	UM0078C-UM0078D	UM0098C-UM0098D	UM00B8C-UM00B8D
Buffer 7	UM0058E-UM0058F	UM0078E-UM0078F	UM0098E-UM0098F	UM00B8E-UM00B8F
Buffer 8	UM00590-UM00591	UM00790-UM00791	UM00990-UM00991	UM00B90-UM00B91
Buffer 9	UM00592-UM00593	UM00792-UM00793	UM00992-UM00993	UM00B92-UM00B93
Buffer 10	UM00594-UM00595	UM00794-UM00795	UM00994-UM00995	UM00B94-UM00B95
Buffer 11	UM00596-UM00597	UM00796-UM00797	UM00996-UM00997	UM00B96-UM00B97
Buffer 12	UM00598-UM00599	UM00798-UM00799	UM00998-UM00999	UM00B98-UM00B99
Buffer 13	UM0059A-UM0059B	UM0079A-UM0079B	UM0099A-UM0099B	UM00B9A-UM00B9B
Buffer 14	UM0059C-UM0059D	UM0079C-UM0079D	UM0099C-UM0099D	UM00B9C-UM00B9D
Buffer 15	UM0059E-UM0059F	UM0079E-UM0079F	UM0099E-UM0099F	UM00B9E-UM00B9F
Buffer 16	UM005A0-UM005A1	UM007A0-UM007A1	UM009A0-UM009A1	UM00BA0-UM00BA1
Buffer 17	UM005A2-UM005A3	UM007A2-UM007A3	UM009A2-UM009A3	UM00BA2-UM00BA3
Buffer 18	UM005A4-UM005A5	UM007A4-UM007A5	UM009A4-UM009A5	UM00BA4-UM00BA5
Buffer 19	UM005A6-UM005A7	UM007A6-UM007A7	UM009A6-UM009A7	UM00BA6-UM00BA7
Buffer 20	UM005A8-UM005A9	UM007A8-UM007A9	UM009A8-UM009A9	UM00BA8-UM00BA9
Buffer 21	UM005AA-UM005AB	UM007AA-UM007AB	UM009AA-UM009AB	UM00BAA-UM00BAB
Buffer 22	UM005AC-UM005AD	UM007AC-UM007AD	UM009AC-UM009AD	UM00BAC-UM00BAD
Buffer 23	UM005AE-UM005AF	UM007AE-UM007AF	UM009AE-UM009AF	UM00BAE-UM00BAF
Buffer 24	UM005B0-UM005B1	UM007B0-UM007B1	UM009B0-UM009B1	UM00BB0-UM00BB1
Buffer 25	UM005B2-UM005B3	UM007B2-UM007B3	UM009B2-UM009B3	UM00BB2-UM00BB3
Buffer 26	UM005B4-UM005B5	UM007B4-UM007B5	UM009B4-UM009B5	UM00BB4-UM00BB5
Buffer 27	UM005B6-UM005B7	UM007B6-UM007B7	UM009B6-UM009B7	UM00BB6-UM00BB7
Buffer 28	UM005B8-UM005B9	UM007B8-UM007B9	UM009B8-UM009B9	UM00BB8-UM00BB9
Buffer 29	UM005BA-UM005BB	UM007BA-UM007BB	UM009BA-UM009BB	UM00BBA-UM00BBB
Buffer 30	UM005BC-UM005BD	UM007BC-UM007BD	UM009BC-UM009BD	UM00BBC-UM00BBD

(Note 1) The capture value buffer areas are available from the high-speed counter unit Ver.1.2.

(Note 2) In the above areas, the capture register difference values (Capture 1 register 1 - Capture 0 register) are stored when capturing for the capture 1 register is executed.

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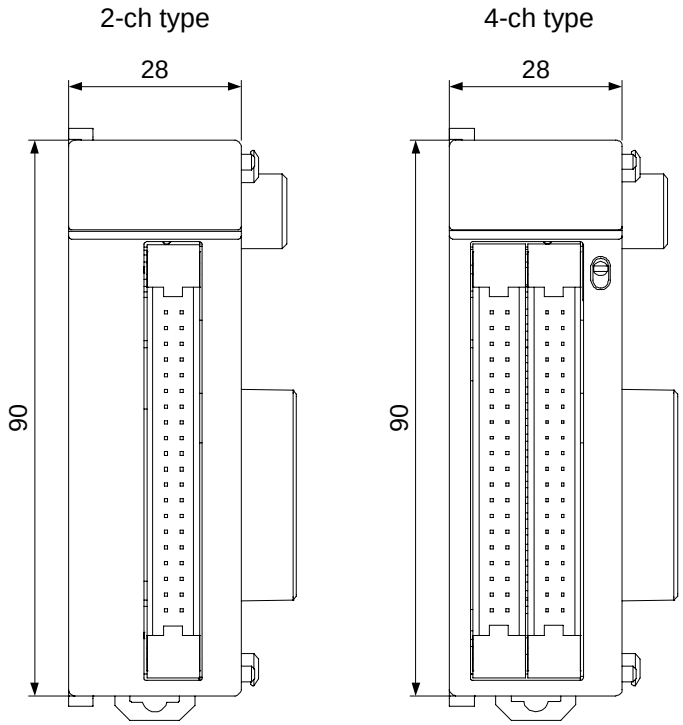
■ **Check list of unit memories (Difference value buffer: Stored when Capture 1 request occurs.)**

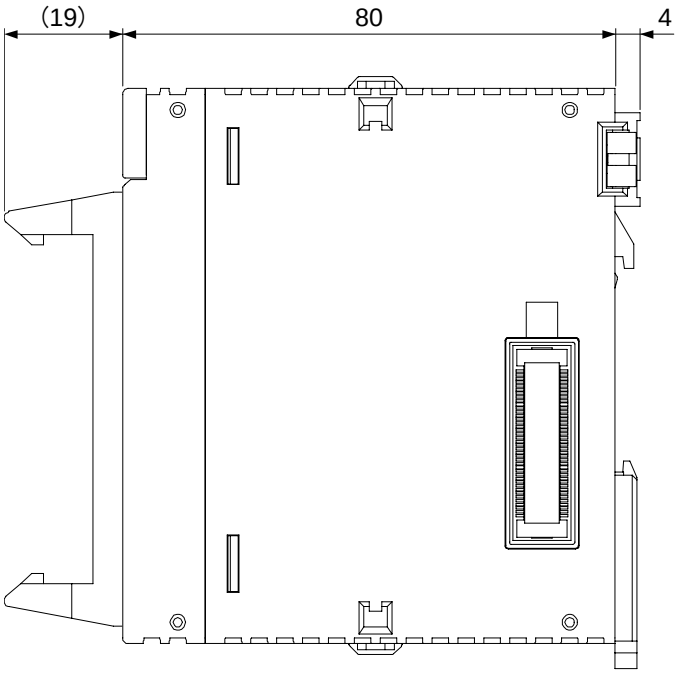
Buffer No.	Unit memory (UM) No.			
	CH0	CH1	CH2	CH3
Buffer 31	UM005BE-UM005BF	UM007BE-UM007BF	UM009BE-UM009BF	UM00BBE-UM00BBF
Buffer 32	UM005C0-UM005C1	UM007C0-UM007C1	UM009C0-UM009C1	UM00BC0-UM00BC1
Buffer 33	UM005C2-UM005C3	UM007C2-UM007C3	UM009C2-UM009C3	UM00BC2-UM00BC3
Buffer 34	UM005C4-UM005C5	UM007C4-UM007C5	UM009C4-UM009C5	UM00BC4-UM00BC5
Buffer 35	UM005C6-UM005C7	UM007C6-UM007C7	UM009C6-UM009C7	UM00BC6-UM00BC7
Buffer 36	UM005C8-UM005C9	UM007C8-UM007C9	UM009C8-UM009C9	UM00BC8-UM00BC9
Buffer 37	UM005CA-UM005CB	UM007CA-UM007CB	UM009CA-UM009CB	UM00BCA-UM00BCB
Buffer 38	UM005CC-UM005CD	UM007CC-UM007CD	UM009CC-UM009CD	UM00BCC-UM00BCD
Buffer 39	UM005CE-UM005CF	UM007CE-UM007CF	UM009CE-UM009CF	UM00BCE-UM00BCF
Buffer 40	UM005D0-UM005D1	UM007D0-UM007D1	UM009D0-UM009D1	UM00BD0-UM00BD1
Buffer 41	UM005D2-UM005D3	UM007D2-UM007D3	UM009D2-UM009D3	UM00BD2-UM00BD3
Buffer 42	UM005D4-UM005D5	UM007D4-UM007D5	UM009D4-UM009D5	UM00BD4-UM00BD5
Buffer 43	UM005D6-UM005D7	UM007D6-UM007D7	UM009D6-UM009D7	UM00BD6-UM00BD7
Buffer 44	UM005D8-UM005D9	UM007D8-UM007D9	UM009D8-UM009D9	UM00BD8-UM00BD9
Buffer 45	UM005DA-UM005DB	UM007DA-UM007DB	UM009DA-UM009DB	UM00BDA-UM00BDB
Buffer 46	UM005DC-UM005DD	UM007DC-UM007DD	UM009DC-UM009DD	UM00BDC-UM00BDD
Buffer 47	UM005DE-UM005DF	UM007DE-UM007DF	UM009DE-UM009DF	UM00BDE-UM00BDF
Buffer 48	UM005E0-UM005E1	UM007E0-UM007E1	UM009E0-UM009E1	UM00BE0-UM00BE1
Buffer 49	UM005E2-UM005E3	UM007E2-UM007E3	UM009E2-UM009E3	UM00BE2-UM00BE3
Buffer 50	UM005E4-UM005E5	UM007E4-UM007E5	UM009E4-UM009E5	UM00BE4-UM00BE5
Buffer 51	UM005E6-UM005E7	UM007E6-UM007E7	UM009E6-UM009E7	UM00BE6-UM00BE7
Buffer 52	UM005E8-UM005E9	UM007E8-UM007E9	UM009E8-UM009E9	UM00BE8-UM00BE9
Buffer 53	UM005EA-UM005EB	UM007EA-UM007EB	UM009EA-UM009EB	UM00BEA-UM00BEB
Buffer 54	UM005EC-UM005ED	UM007EC-UM007ED	UM009EC-UM009ED	UM00BEC-UM00BED
Buffer 55	UM005EE-UM005EF	UM007EE-UM007EF	UM009EE-UM009EF	UM00BEE-UM00BEF
Buffer 56	UM005F0-UM005F1	UM007F0-UM007F1	UM009F0-UM009F1	UM00BF0-UM00BF1
Buffer 57	UM005F2-UM005F3	UM007F2-UM007F3	UM009F2-UM009F3	UM00BF2-UM00BF3
Buffer 58	UM005F4-UM005F5	UM007F4-UM007F5	UM009F4-UM009F5	UM00BF4-UM00BF5
Buffer 59	UM005F6-UM005F7	UM007F6-UM007F7	UM009F6-UM009F7	UM00BF6-UM00BF7
Buffer 60	UM005F8-UM005F9	UM007F8-UM007F9	UM009F8-UM009F9	UM00BF8-UM00BF9

(Note 1) The capture value buffer areas are available from the high-speed counter unit Ver.1.2.

(Note 2) In the above areas, the capture register difference values (Capture 1 register 1 - Capture 0 register) are stored when capturing for the capture 0 register is executed.

11.5 Dimensions





Record of changes

Manual No.	Date	Record of Changes
WUME-FP7HSC-01	Oct.2013	First Edition
WUME-FP7HSC-02	Jun.2014	Second Edition Specification change: Capture function (Chapter 4.1, Chapter 8, Chapter 11.2 to 11.4) Correction of sample programs related to "Operation Ready Request" and "Configuration Using User Programs" (Chapter 4.3, 4.4)

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